Programmable Trigger Board and Mean Timer(BNL-E949)

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Contents

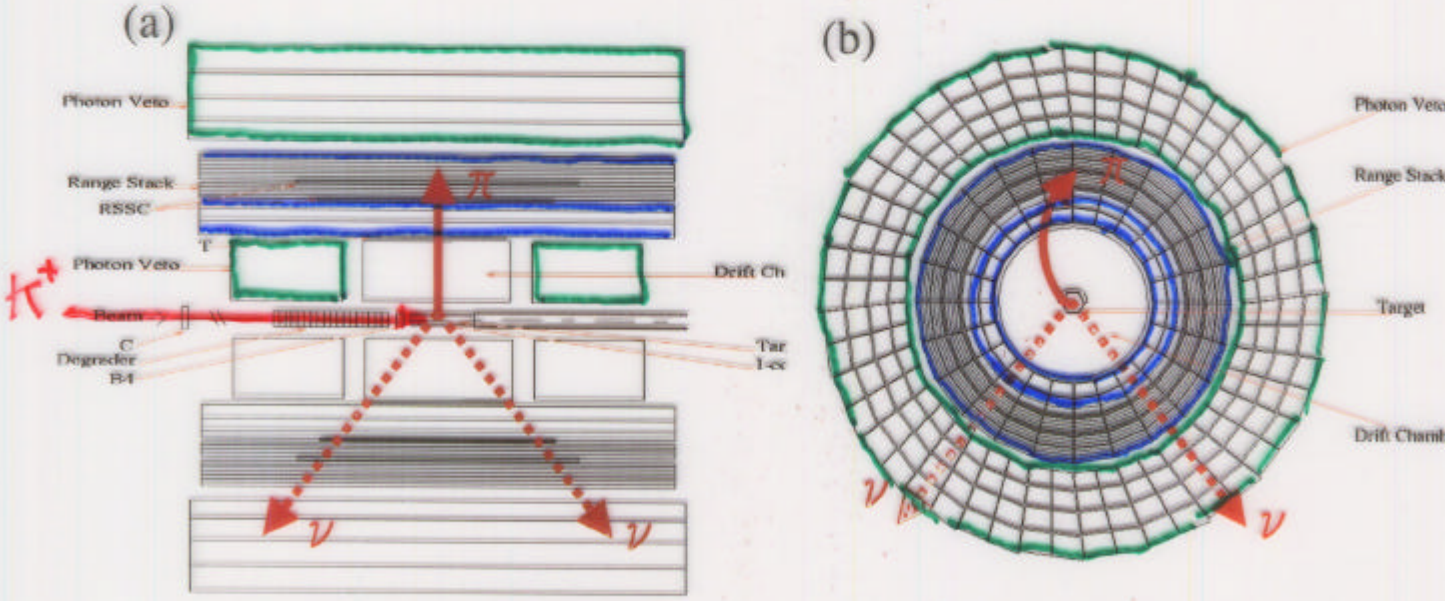
1. E949 Detector and Trigger

$\pi^+ \nu \bar{\nu}$ trigger

$KB \cdot DC \cdot (T \cdot 2) \cdot (6_{ct} + 7_{ct}) \cdot \overline{19_{ct}} \cdot \overline{(BV+EC)}$

$\cdot$Refined Range $\cdot$HEX $\cdot$L1.N

- Level 0 Trigger Board execute the trigger logic which is described as AND/OR of trigger signals.
- There are several monitor triggers for the purpose of calibrations.



Top half of side(a) and end(b) view of the E949 detector

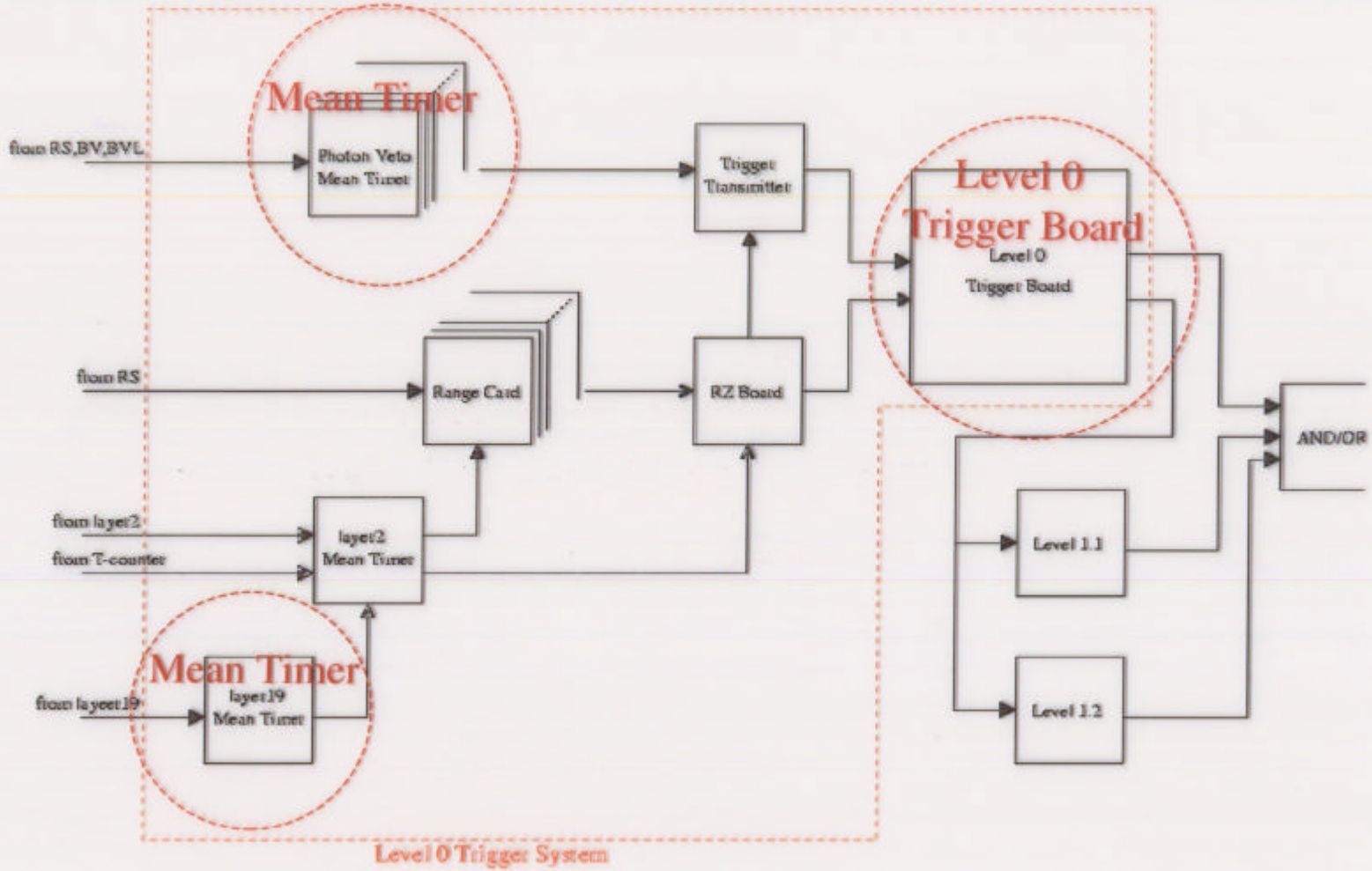
2. Motivation

The development of the trigger system is necessary to deal with the high intensity beam.

Level 0 Trigger Board and Mean Timer module with Programmable Logic Device(PLD) are introduced newly in the E949 experiment.

- Prototype module is made and tested.

E949 trigger system

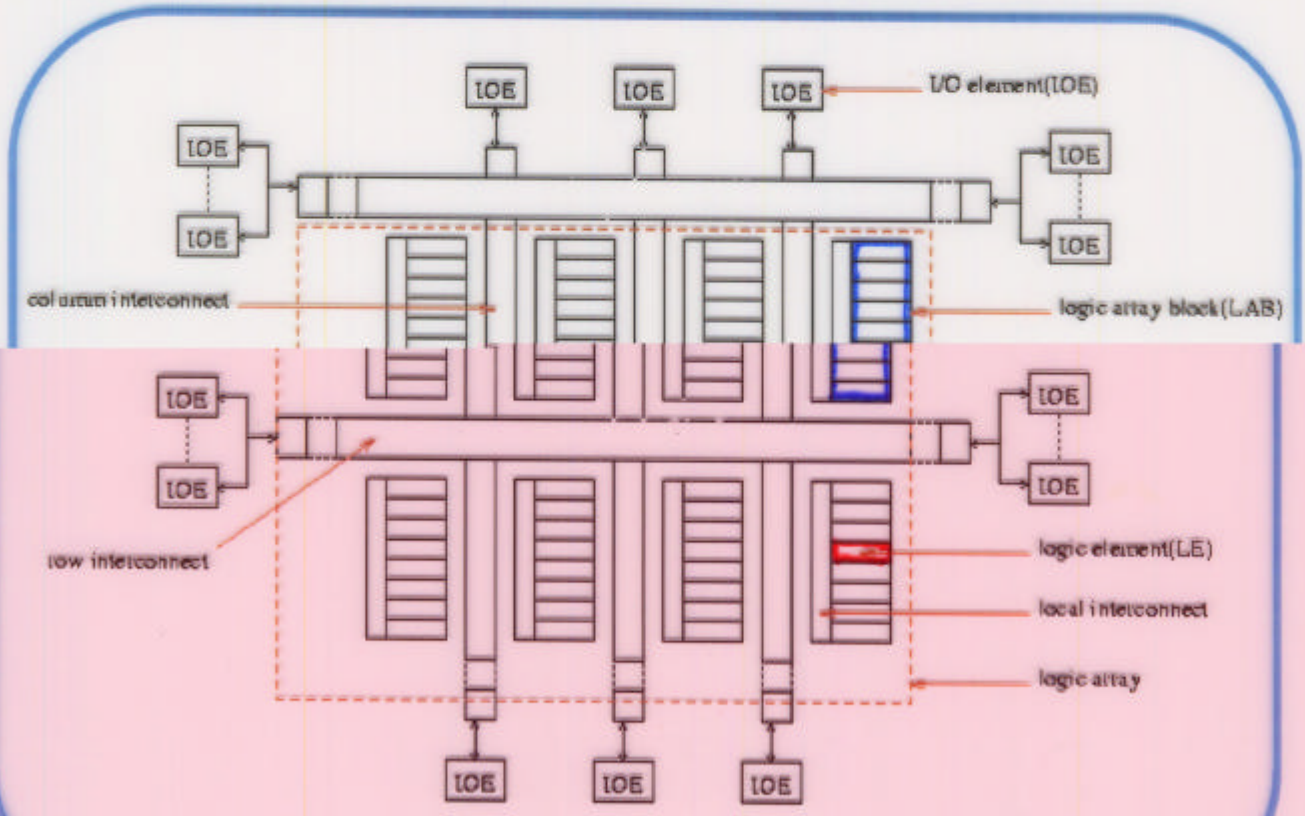


Level 0 online dead time : ~40nsec

Level 0 rejection : 550 ~750

ALTERA
Programmable Logic Device

- A Logic which is described to Hardware Description Language(HDL) can be down loaded from PC.
- There are FLEX devices and MAX devices in ALTERA PLD.
- Down loaded through JTAG link.



Block diagram of FLEX device

3. Level 0 Trigger Board

·E787 Trigger Board(Old)

·Wire-wrapped board.

·Hard to maintenance.

·4 FUSTBUS boards.

·E949 Trigger Board(New)

·Execute triggers in a PLD.

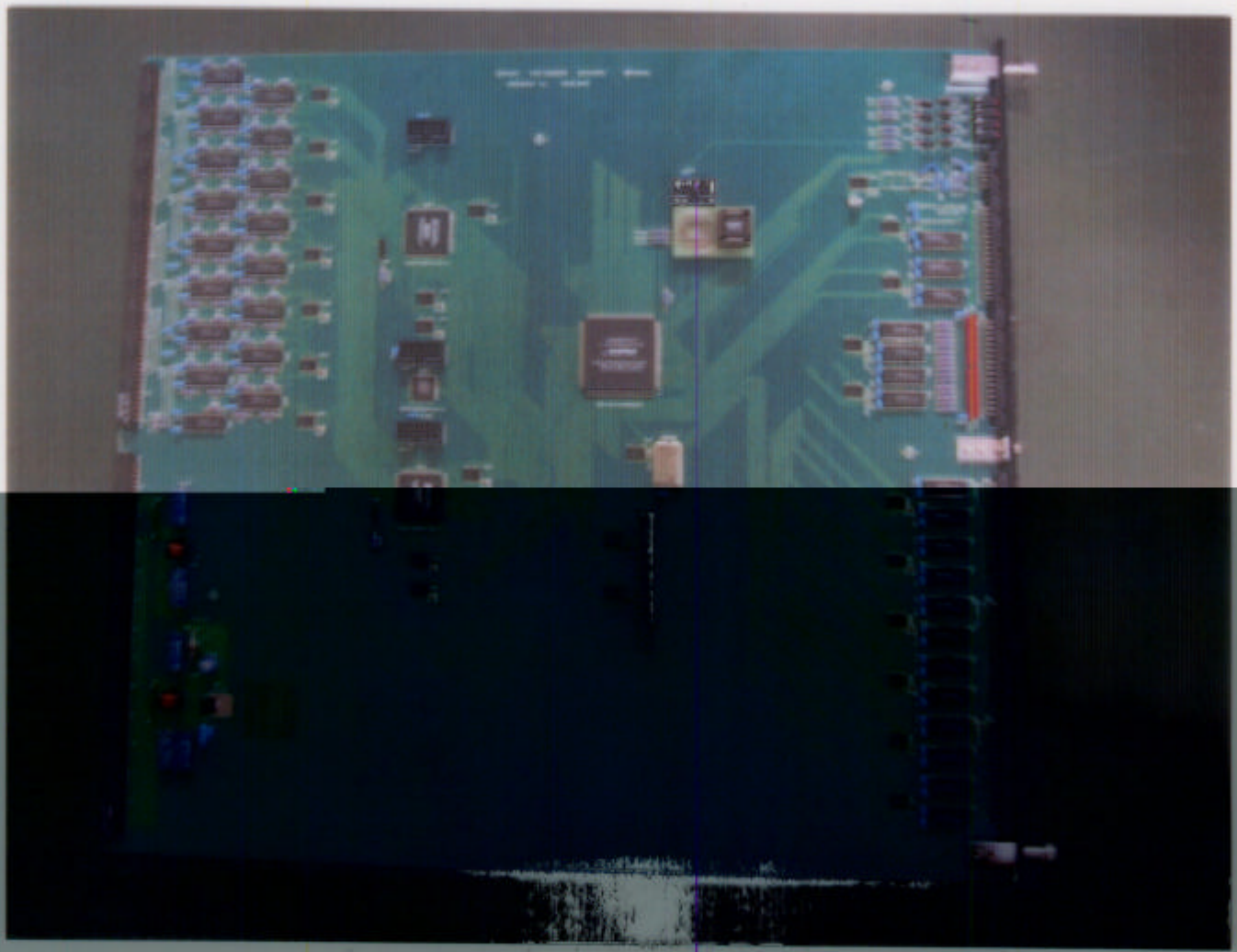
·Easy to maintenance.

·1 FUSTBUS board.

·Propagation time through on the board must to be within 19nsec.

Level 0 Trigger Board prototype

- FASTBUS board.
- FLEX10K100E device and MAX7128B devices.
- ECL/TTL,TTL/ECL conversion.
- 65 inputs in FASTBUS P1connector.
- 80MHz clock.



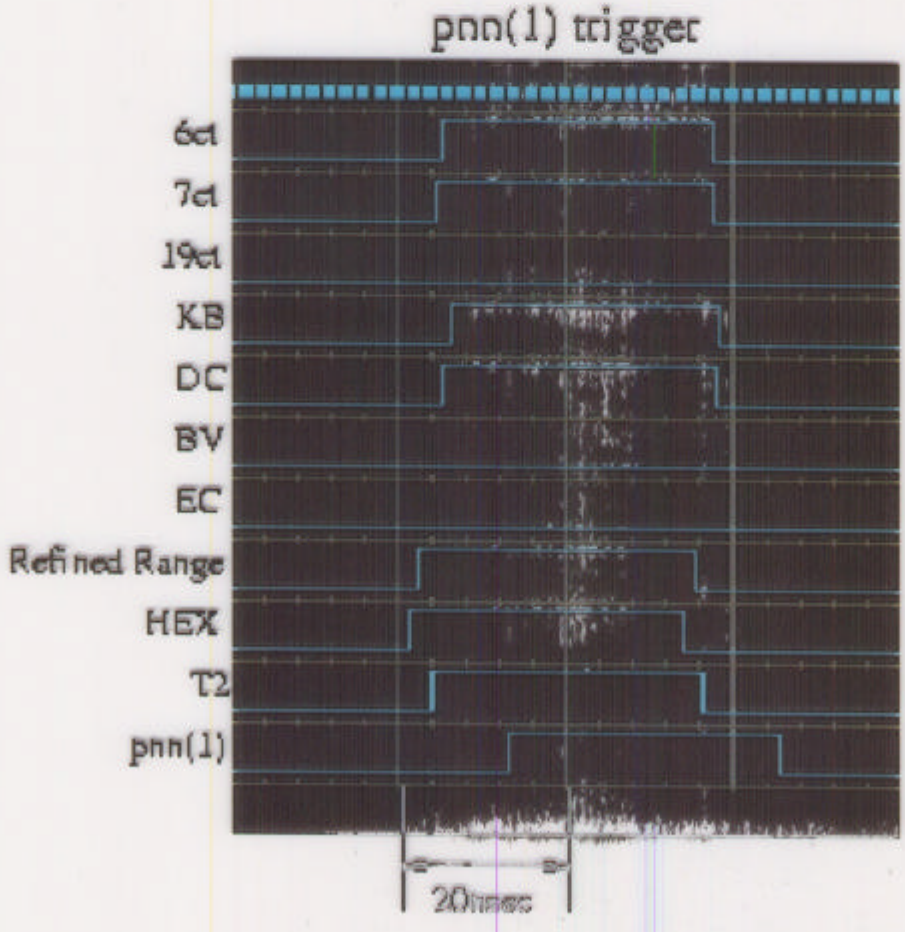
Logic Test

$\pi^+ \nu\ \bar{\nu}$ level 0 trigger

$$KB \cdot DC \cdot (T \cdot 2) \cdot (6_{ct} + 7_{ct}) \cdot \overline{19_{ct}} \cdot \overline{(BV+EC)} \cdot \text{Refined Range} \cdot HEX$$

· propagation time of the prototype board

ECL/TTL,TTL/ECL conversion	8nsec
PLD(MAX)	8nsec
Propagation on board	2nsec
Total	18nsec



4. Mean Timer module

It is introduced newly in the E949 experiment.

·Photon Veto Mean Timer

·Mean Timing the RS,BV,BVL counter.

·Reduce accidental veto rate.

Time window 21nsec → 5～6nsec

·T·2 Veto Mean Timer

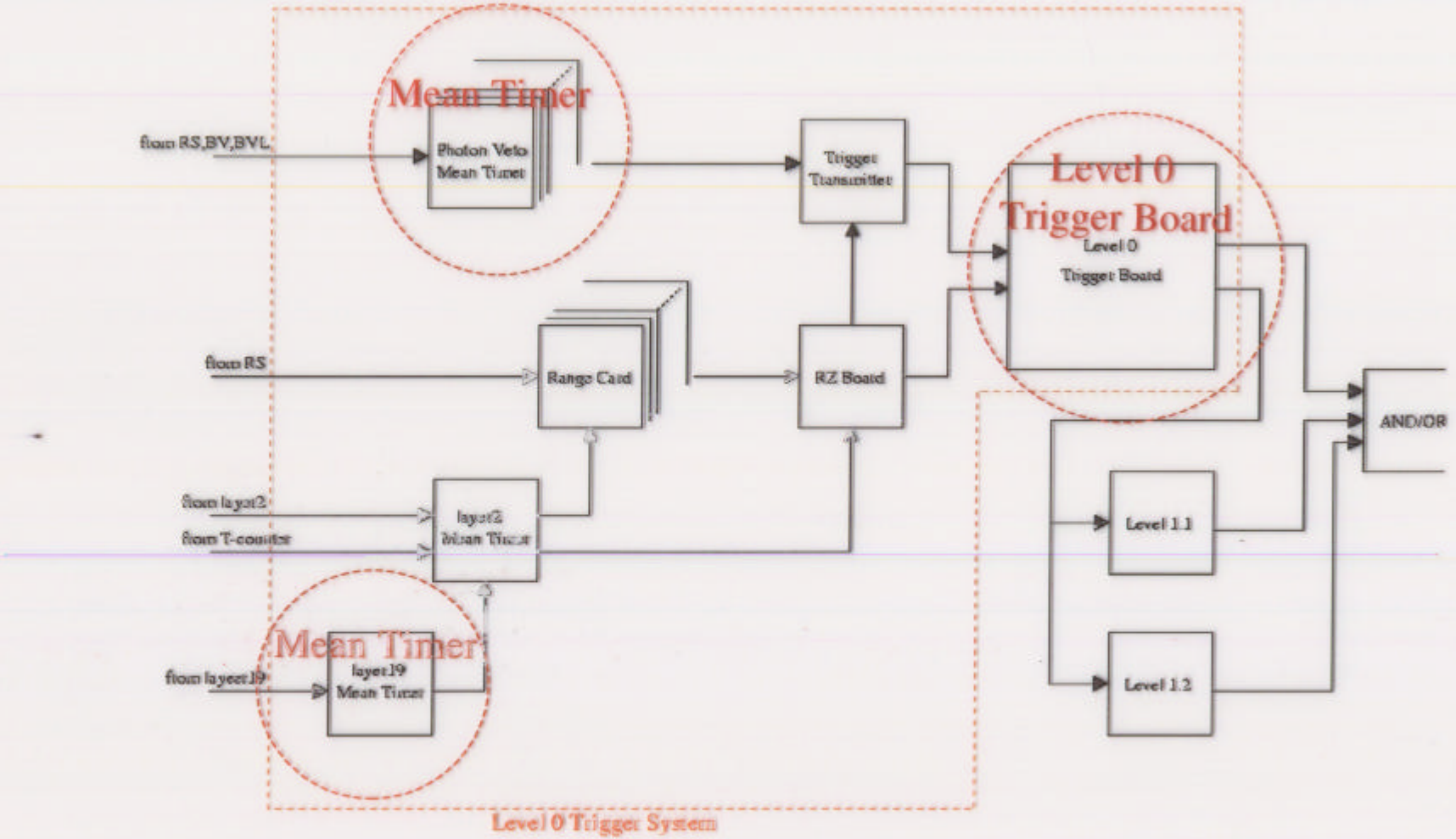
·Mean Timing the RS layer19 counter.

·Reduce the T·2 signal rate.

→ Reduce the Level 0 Trigger dead time.

·K→ μ ν event can be removed at the early stage.

E949 trigger system

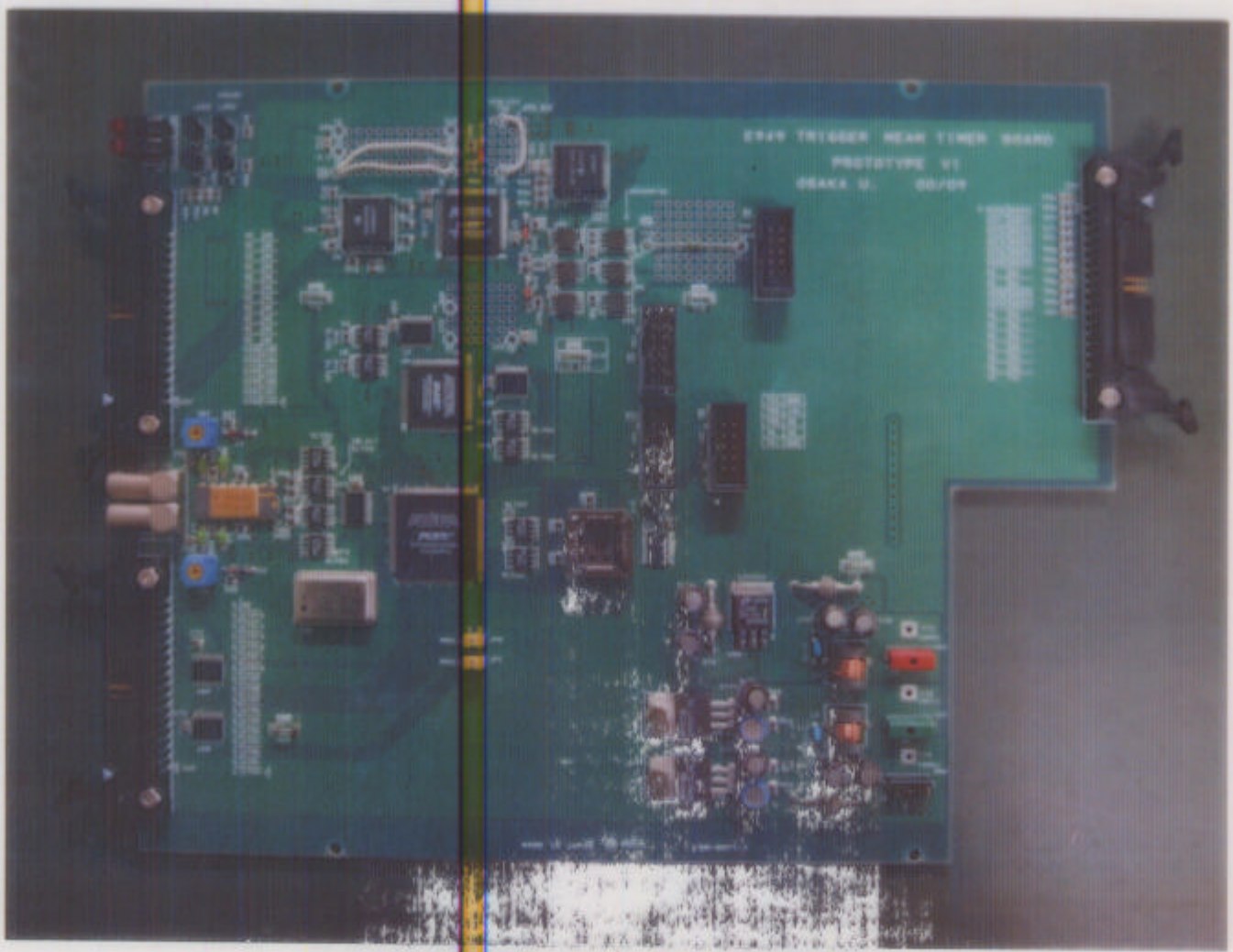


Level 0 online dead time : ～40nsec(25MHz)

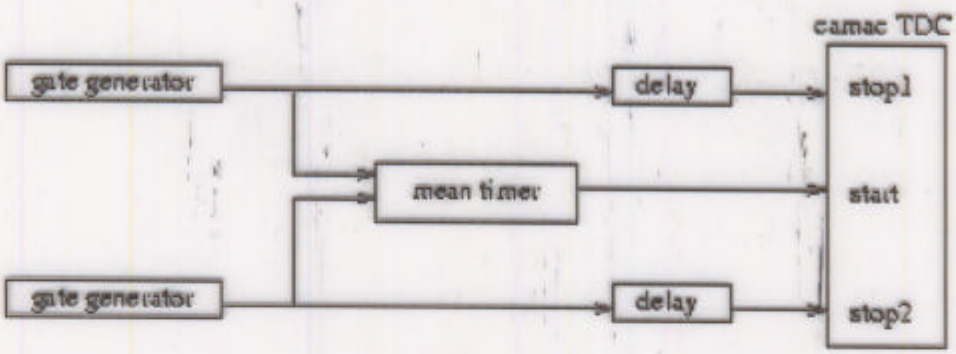
Level 0 rejection : 550 ～750

Mean Timer module prototype

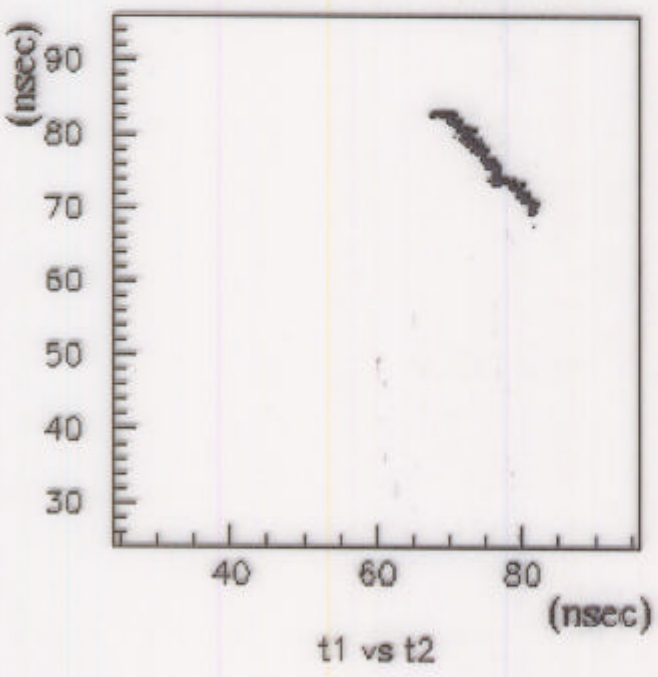
- FLEX10K30E(propagation time of one delay-cell ~ 1nsec).
- Discriminator chip(SPT9689).
- ECL/TTL,TTL/ECL conversion.



Mean Timer performance

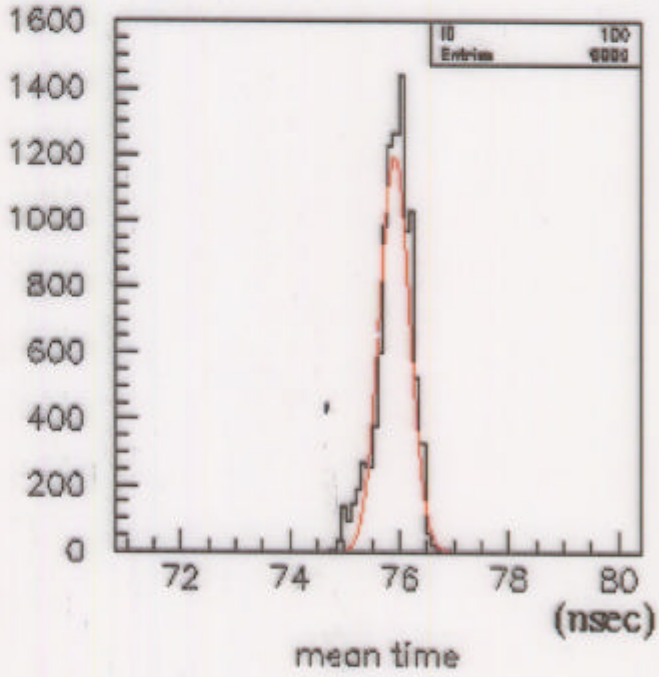


·Generate mean time signal from two random signals



t1 vs t2

delay-line 12cell



(t1+t2)/2

RMS=0.27nsec

result

5. Summary and Future

Level 0 Trigger Board

- Propagation time of the prototype board is less than 19nsec.
- Prototype board is good.

Mean Timer module

- Design of the prototype board is fine.
- PLD Mean Timer : RMS = 0.27nsec.

Future plans

- Further tests will be done at BNL in Feb.
- Final modules will be ready by the end of April.
- Start physics run in Summer.

MAX+plus2 floor editor plan