Electronics modules & DAQ system

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1. Front-end studies
2. Read-out platform
3. Back-end system
4. Signal handling
5. Summary

COLLABORATION

KEK online/electronics group
Belle DAQ group
KEK Neutrino DAQ group
Hiroshima Institute of Technology
University of Hawaii
University Tokyo
BINP(Budker Institute of Nuclear Physics)
KRAKOW Institute of Nuclear Physics
Densan Co. Ltd.
Designtech Co. Ltd

Requirements of electronics systems for J-PARC experiments

- Trigger : 数 KHz
- Data flow : 数十 MB/sec
- 保守コストの削減
  - Customize/development/upgrade
- 使用にあまり特別な知識を要しない。
- 過去の資産との共存。

CAMAC	あまり速度が出ない、チャンネル密度が上がらない。
TKO	~300 μsec 以上の dead-time、保守コストが高い。
FastBus	消費電力が大きい、新規モジュールの入手が出来ない。
VME Compact PCI	ほとんどディジタル回路専用、アナログ信号を扱うのが難しい(負電源、電源のノイズ)

New front-end system.

Front-End Studies

- Required Readout System
  - General (DC, MWPC,…)
    - Timing resolution : ~1nsec
    - Analog dynamic range <12 bit
  - Wide dynamic range waveform sampling (CsI(Tl),…)
    - Timing resolution : A few hundred nsec
    - Analog dynamic range : 16~18bit
    - Wave form sampling
  - High timing resolution (TOF)
    - Timing resolution : <50 psec
  - High density device
    - Silicon micro-strip detector
    - Multi-anode PMT

•TMC + ADC
•Waveform sampler

Multi Stage Amp
+ Flash ADC

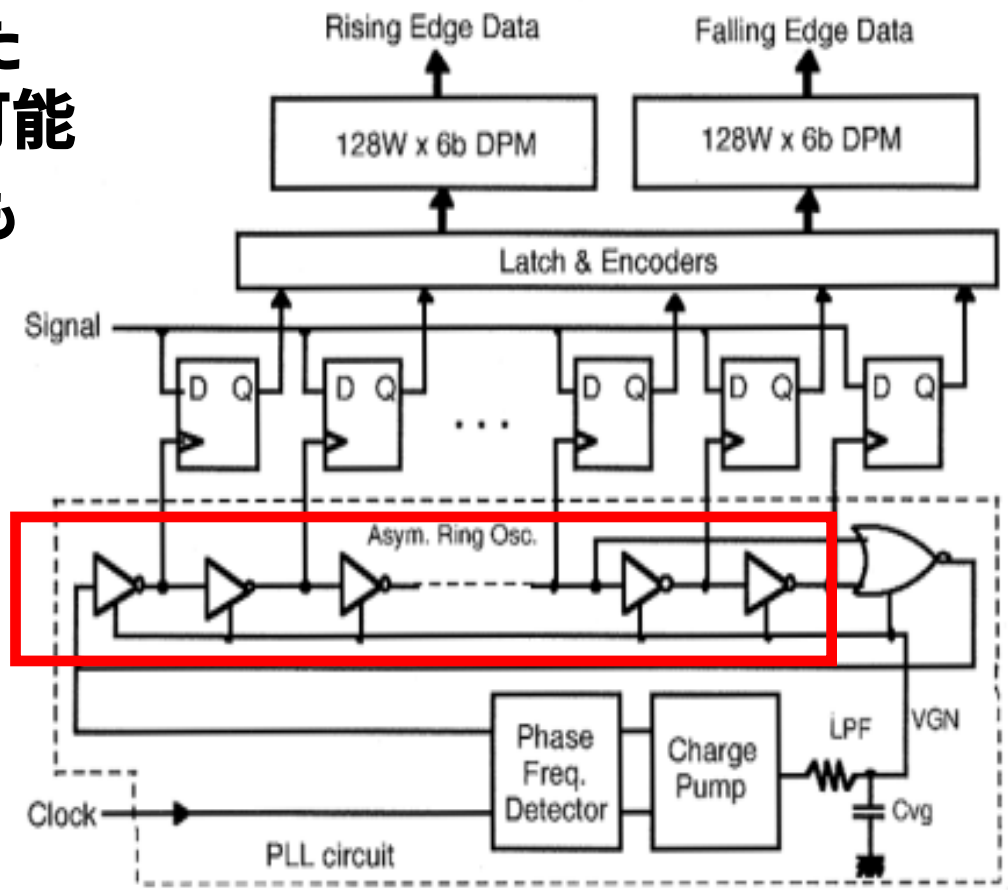
High-resolution TMC

Time-stretcher + TMC

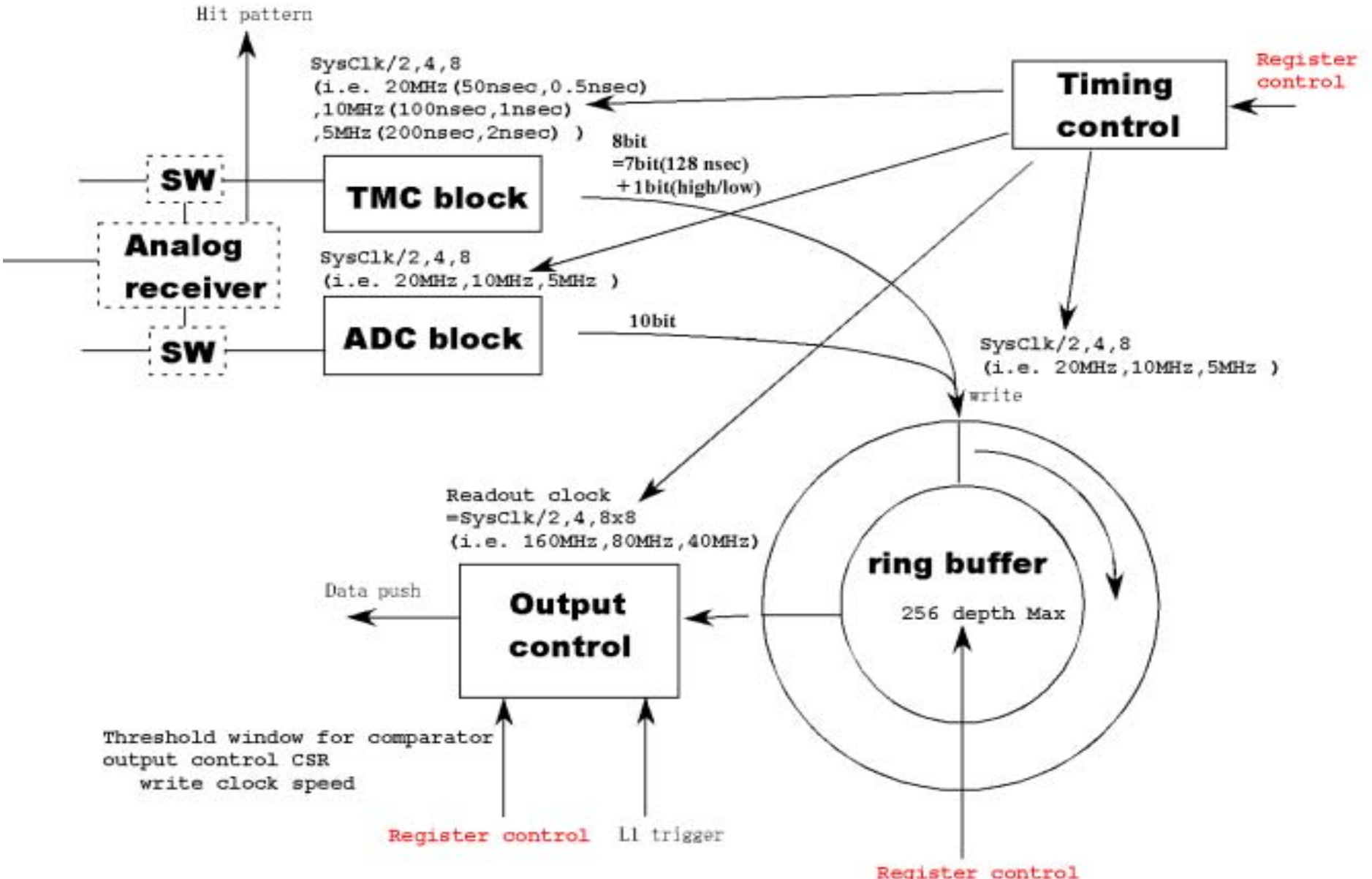
•VA-TA + Flash ADC
•New Front-end ASIC

TMC (Time Memory Cell)

- Logic cell delay を利用した時間測定。
  - ATLAS用に開発された AMT2,AMT3 が入手可能
  - KEK 回路グループでも開発/試作中



TMC/ADC multi-function device

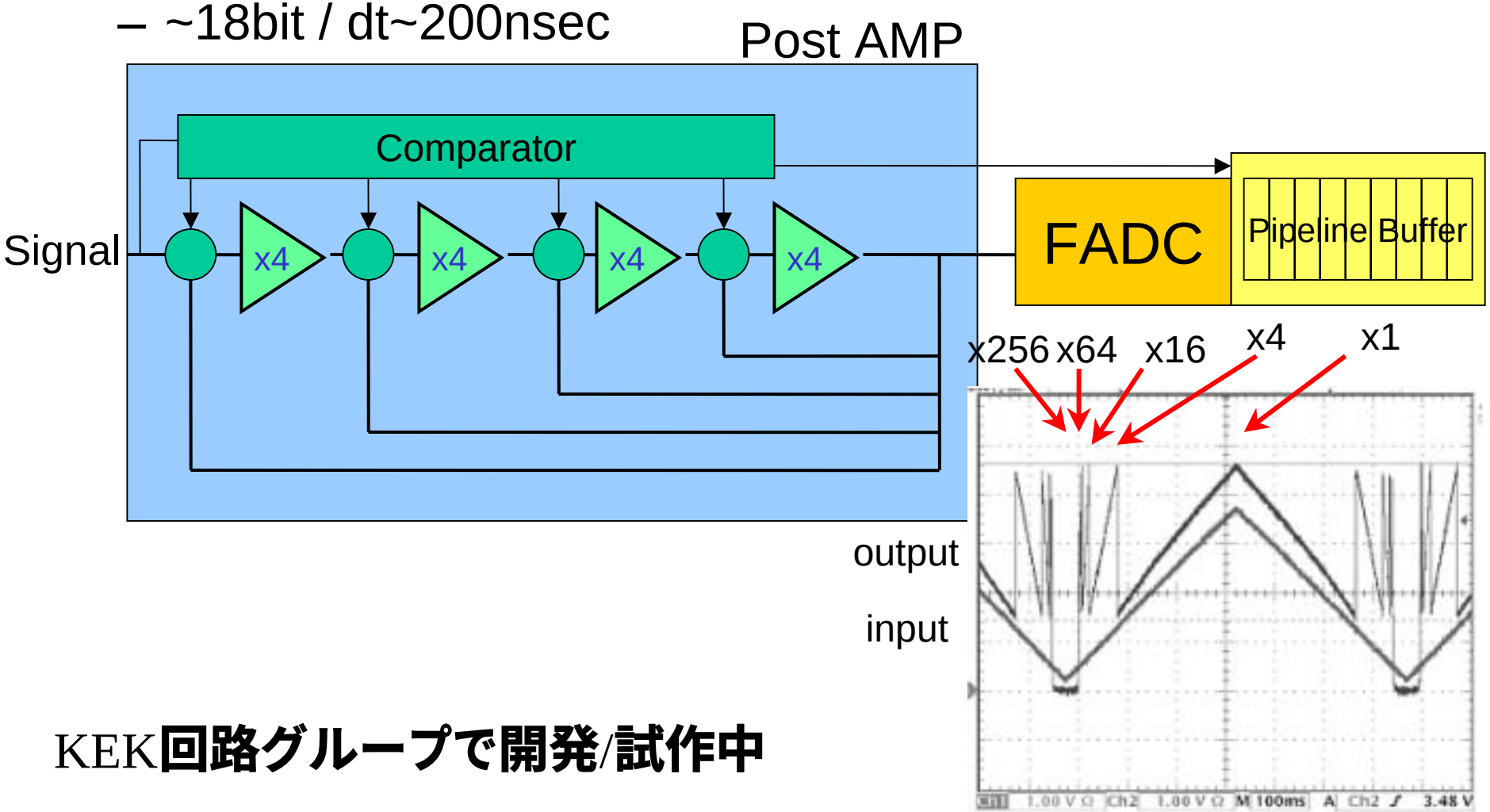


TMC/ADC specification

# of channels (ch/chip)	8 ch/chip
System clock	< 45MHz
ADC sampling rate	< 22MHz selectable SysCLK/N (N=2,4,8)
ADC resolution	8 bit < <10 bit
Analog input range	2 V
TMC timing resolution	0.5～2nsec
L1 buffer depth	256 depth (Depth is changed by CSR)
Power supply	3.3～5V
Power dissipation	< ? mW/chip
Input	TDC, ADC

Wide dynamic range waveform sampling

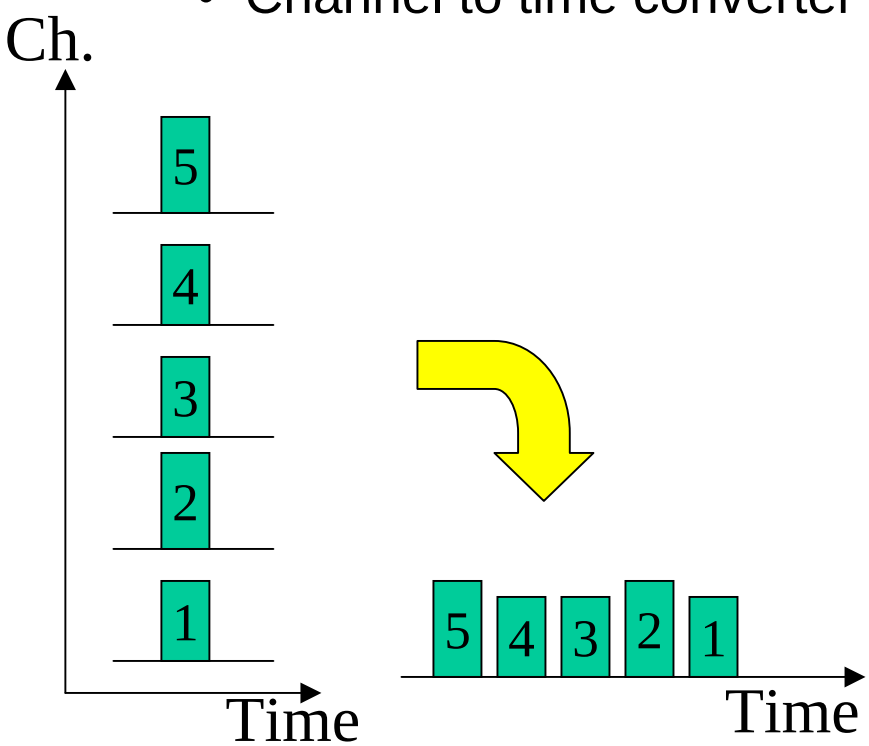
- ASIC Multi Stage Op-amp
  - ~18bit / dt~200nsec



KEK回路グループで開発/試作中

High density devices

- ideas VA-TA
  - Amp/shaper
  - Sample & hold
  - Analog serializer
    - Channel to time converter



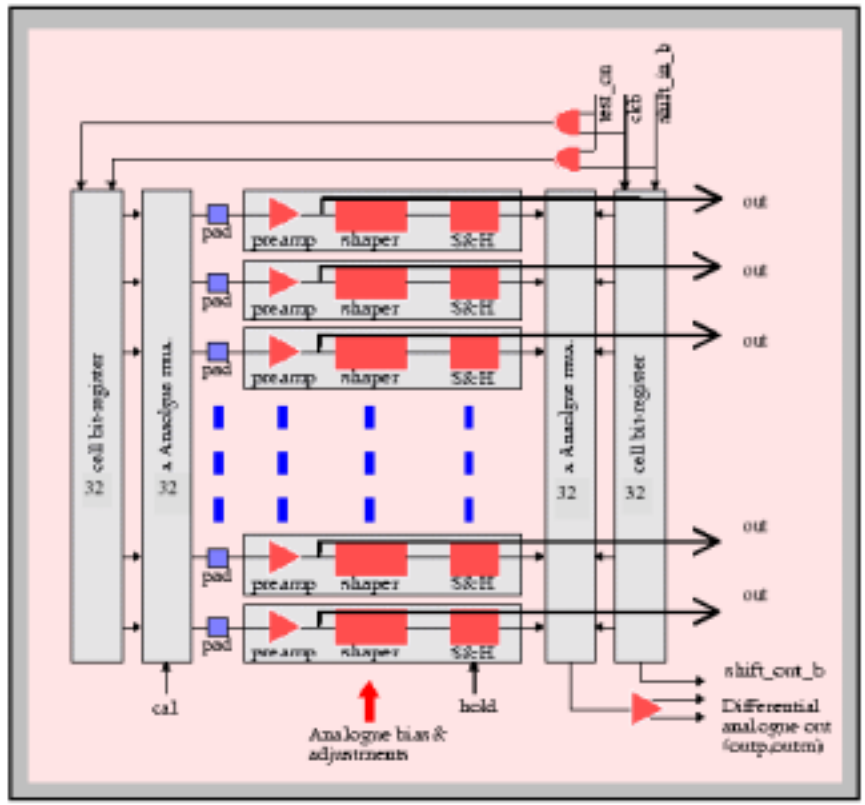


Fig 4. VA32_HDR11 Architecture

- BELLE SVD2, K2K Scibar 検出器で使用中
- より Dead-time の少ないものを ASICで生産できるように研究中

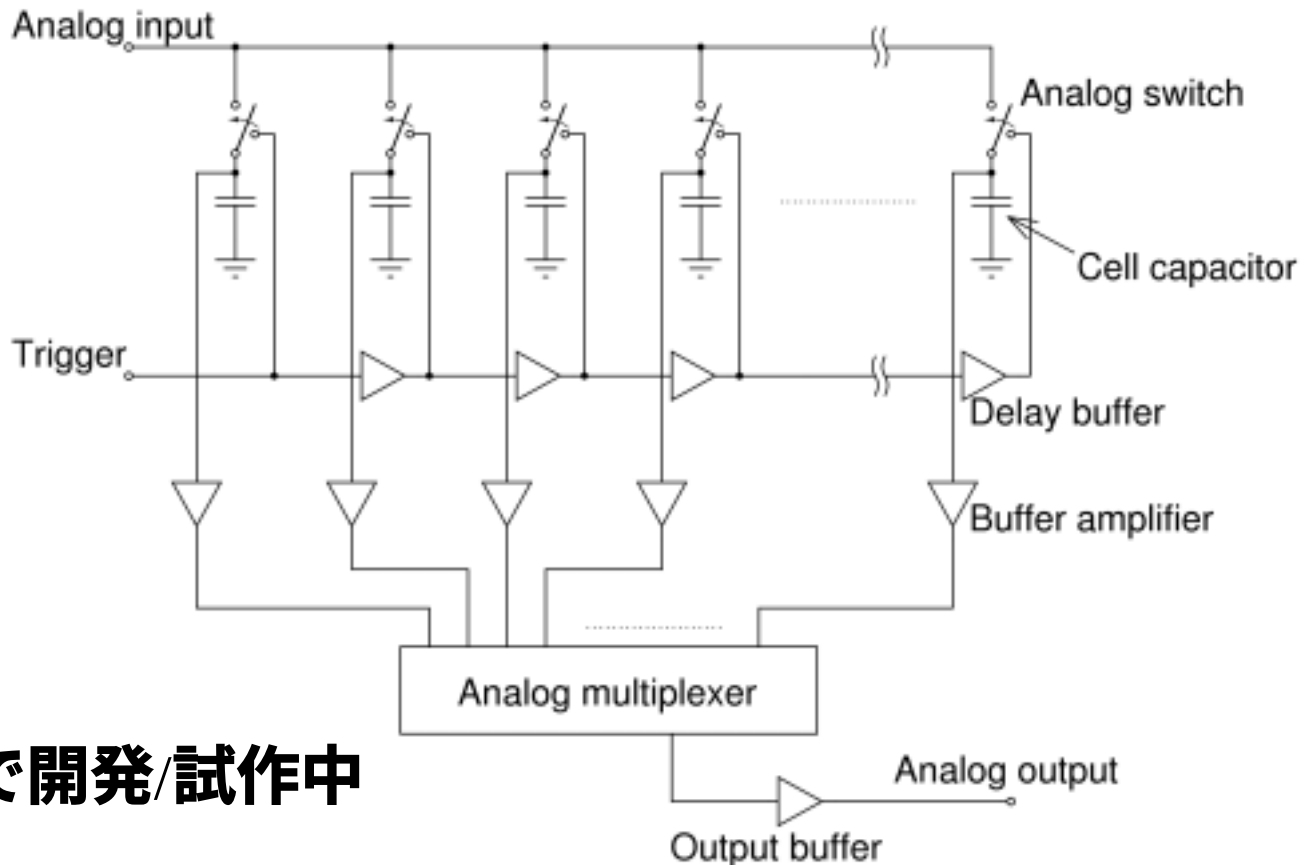
Analog Memory Cell (AMC)

高速クロックなしで1GHz waveform sample **が可能**

(For PMT, Drift chamber)

特徴

- **低コスト**
- **低消費電力**

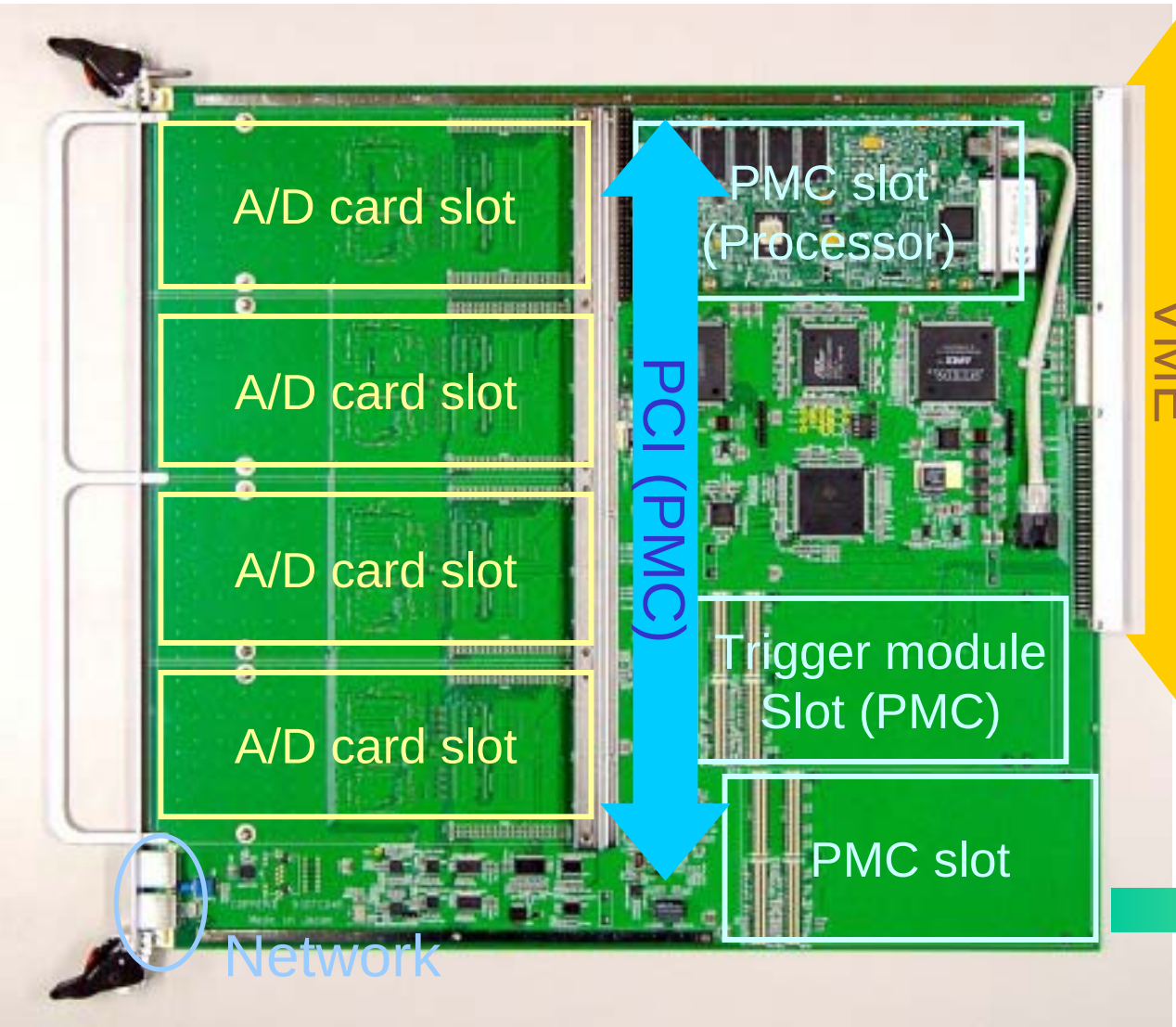


KEK**回路グループで開発/試作中**

Read-out Module design Concept

- Working under 10kHz trigger
  - Front-end Buffering
    - Waiting trigger decision
    - Buffering trigger non-uniform timing
    - Buffering behind non real-time system
  - On-board data reduction
- Wide scalability
  - From small test experiments to large experiments such as Super KEKB experiment
- Modular system
  - Maintenance, upgrading, developing
- Using standard and commercially available technologies
  - Easy to follow evolution of technology
  - Cost effectiveness
    - Production, maintenance, upgrading
- High channel density : ~100 ch/board

Read-out module (COPPER)



- 9U euro card(VME)
- 4 Front-end A/D card slot
- Processor PMC slot
- Trigger module slot
- general PMC slot
- VME-32 interface
- 1MB x 4 FIFO
- 32bit 33MHz PCI bus
- 2 network interface
  - Processor module
  - On-board NIC

PCI / PMC

- PCI Mezzanine Card, IEEE1386.1
  - PCI **互換**
  - **さまざまなモジュールが流通している。**
    - Processor (PPC/x86/…)
    - 100Base/Gigabit Ethernet
    - IEEE1394
    - Memory
    - Etc….

Ramix PMC610
4port Ethernet card

PC architecture / Linux 2.4

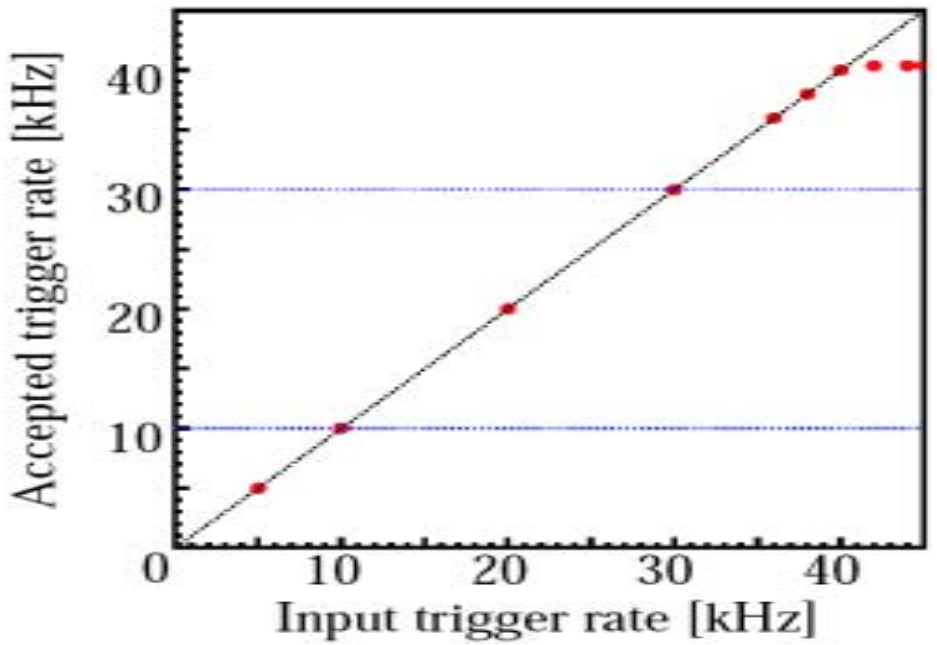
- **研究者がなじんでいる環境。**
  - **普段から解析やメールで使用している。**
  - **プログラムの開発に抵抗が少ない。**
  - **その辺の PC で開発可能。**
- **商業的に成功している**
  - **高速なプロセッサを安く購入できる。**
  - **アップグレードが期待できる。**
- **複雑なデバイスをドライブできる。**
- **いろいろなノウハウが公開されている。**

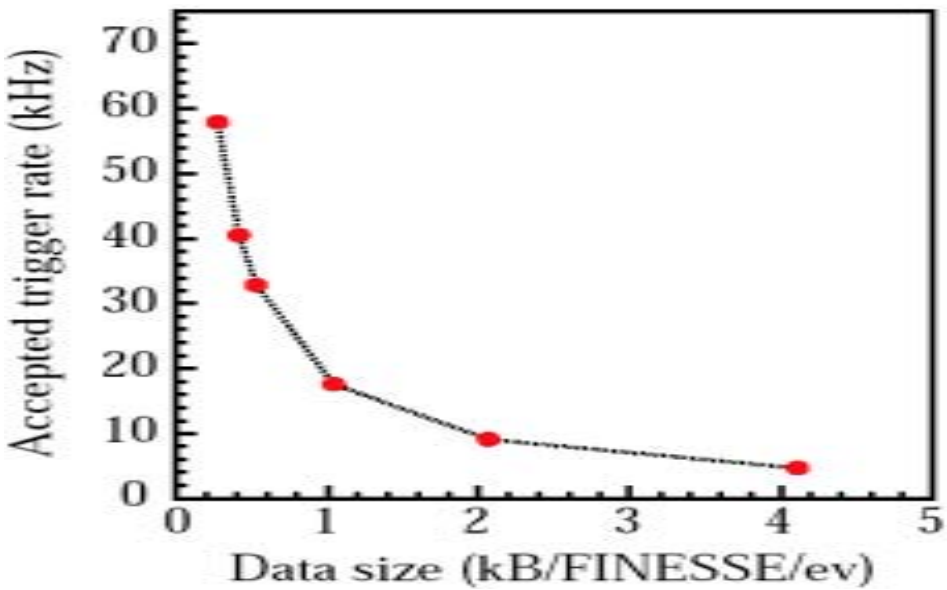
Radisys EPC-6315

- 800 MHz Pentium IIIm Processor.
- Up to 512 MB SDRAM with ECC.
- 10/100 BaseT Ethernet port
- On-board Compact Flash socket.
- 32-bit 33/66 MHz PCI bus interface.

Performance Test

- Data size of this test
  - 400B * 4 = 1600B
- Basic speed of data transfer during DMA cycle
  - ~80MB/sec
- The system works stably.
- Performance limited by processor speed.
  - It can accept more high frequency trigger by more powerful processor.





Front-end daughter card

開発中の Front-end daughter card

- Time Memory Cell (TMC) based pipeline TDC
  - TMC : AMT3
  - Input : 24ch LVDS
  - 96 ch/board
  - Resolution: 0.78 ns/bit
- Flash ADC
  - **8bit/500MHz sample 2ch x 4 FADC**
  - **12bit/65MHz sample 8ch x 4 FADC**

Prototype of flash ADC

- ADC: Analog Devices AD9235-20
- Resolution: 12bit
- Number of channel: 8
- Max sampling clock: 40MHz

計画中の Front-end daughter card

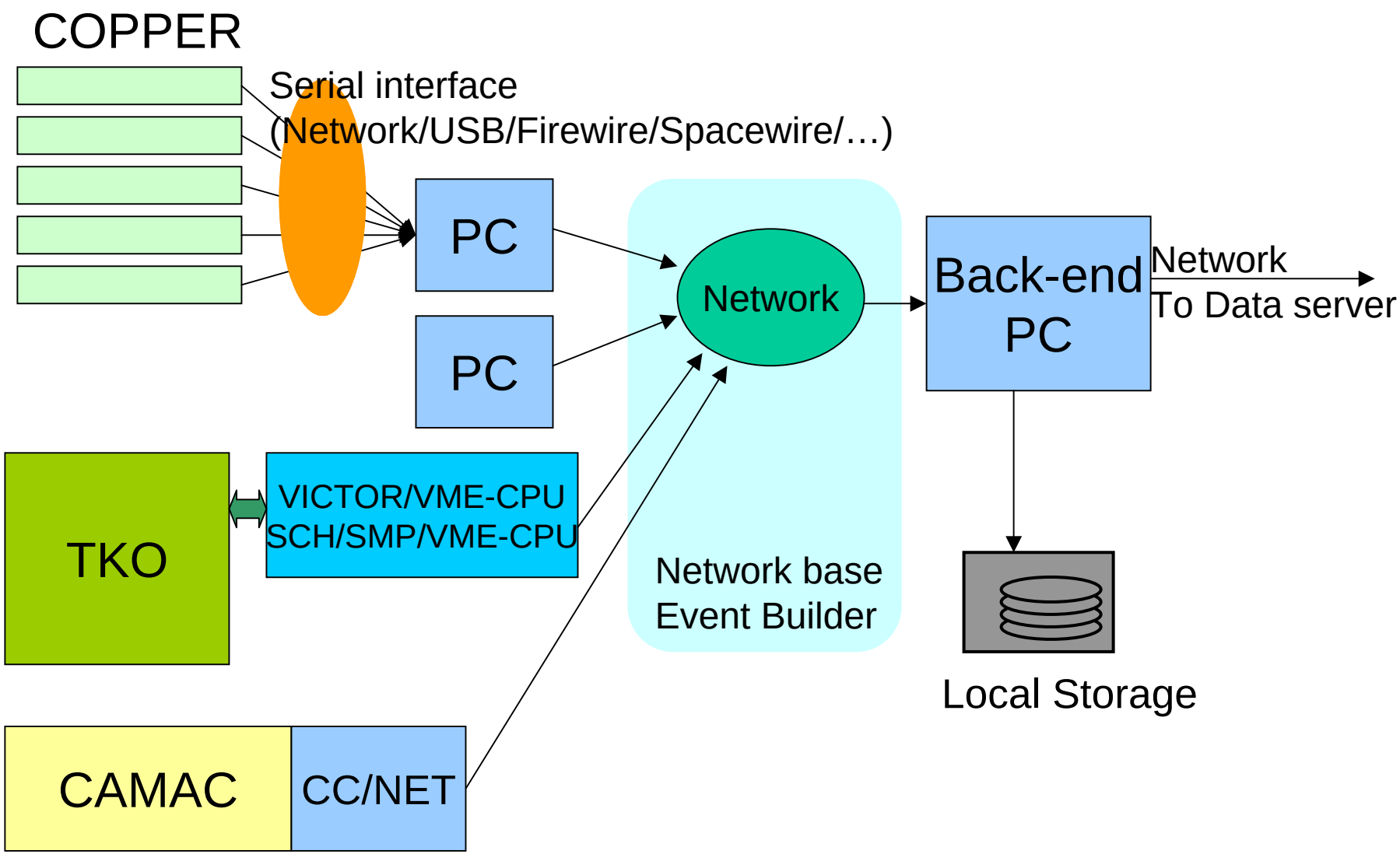
- CCD read-out ADC
- Analog memory cell
  - 1GHz sample
- 16bit wave form sampler
  - 5MHz sample
- High resolution TDC
  - 50psec
- DSSD pipeline front-end (CMS)
- Charge sensitive ADC
  - Current integrator type
  - ASIC

Read-out by CAMAC

- TOYO CC/NET
  - CAMAC crate controller equipped with built-in PC
  - High speed CAMAC ACTION (~1μsec) used by pipe-line architecture
  - Developed by TOYO/Fird/KEK online/elec. Gr.

Built-in PC
- PC104plus
- Crusoe TM5400 500MHz
- Memory 310MB
- Fast Ethernet
- Compact Flash
- …

Data way (Event Builder)



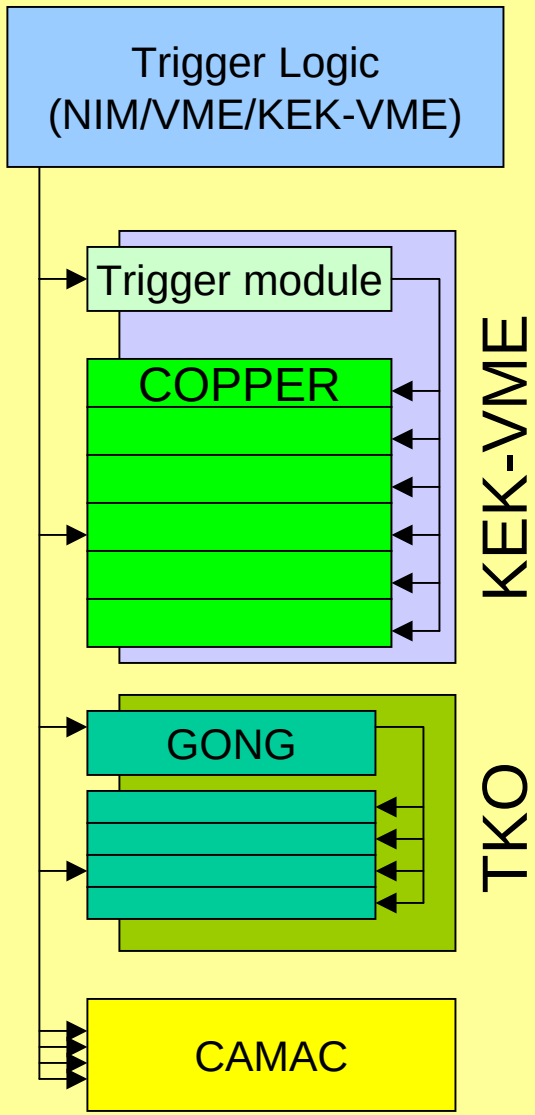
Signal handling tools

- NIM
  - Traditional modules
- KEK-VME (VME + extended power supply + low noise power supply)
  - Read-out module (COPPER)
  - General purpose I/O module
  - Clock Generator
  - Gate Generator
  - Discriminator (under development)

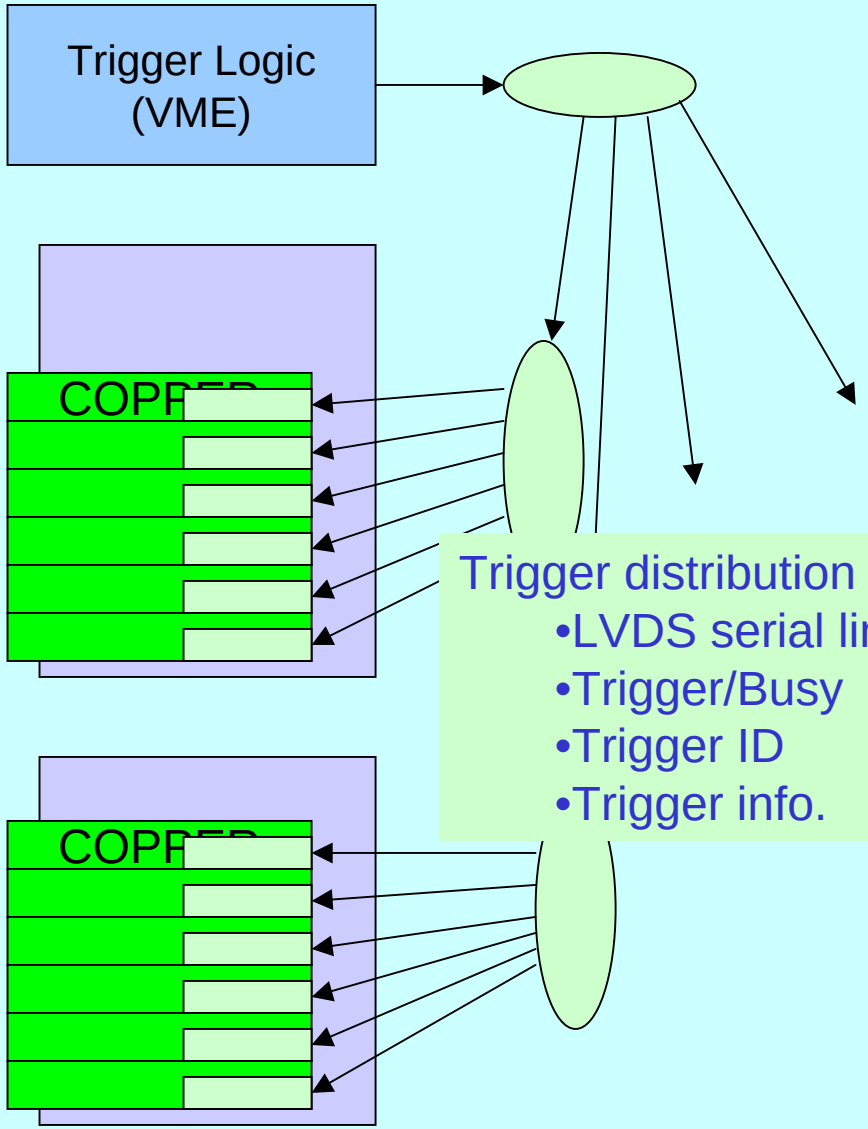
Gate Generator/Clock Generator

General purpose I/O module

Trigger distribution



Simple style



Belle style

まとめ

- **KEK online/electronics gr. では共同研究者の人々と共にの次期実験のために以下のような開発を行っている。**
  - Front-end studies
    - TMC,TMC/ADC multi-function device
    - Multi-stage Amp.
    - VA-TA, New front-end device
    - Analog memory cell
    - ASIC technology
  - Read-out system
    - Read-out platform COPPER
    - CAMAC C.C. CC/NET
  - KEK-VME base signal handling modules
  - Back-end system
    - Network event builder

Appendix

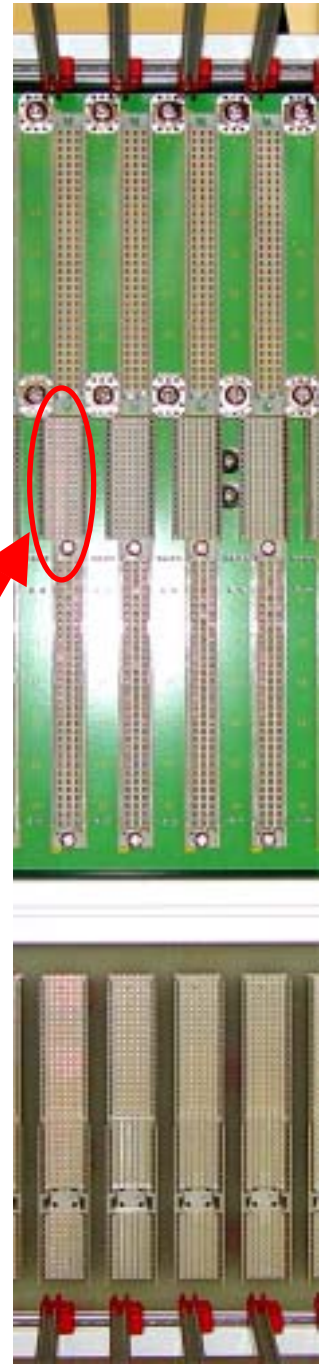
Form Factor and Power Supply

- Euro card/crate
  - Cost effectiveness
  - 9U and 6U
  - VME-32 bus
- J0 Connector for Power Supply
  - To treat front-end analog-digital conversion devices

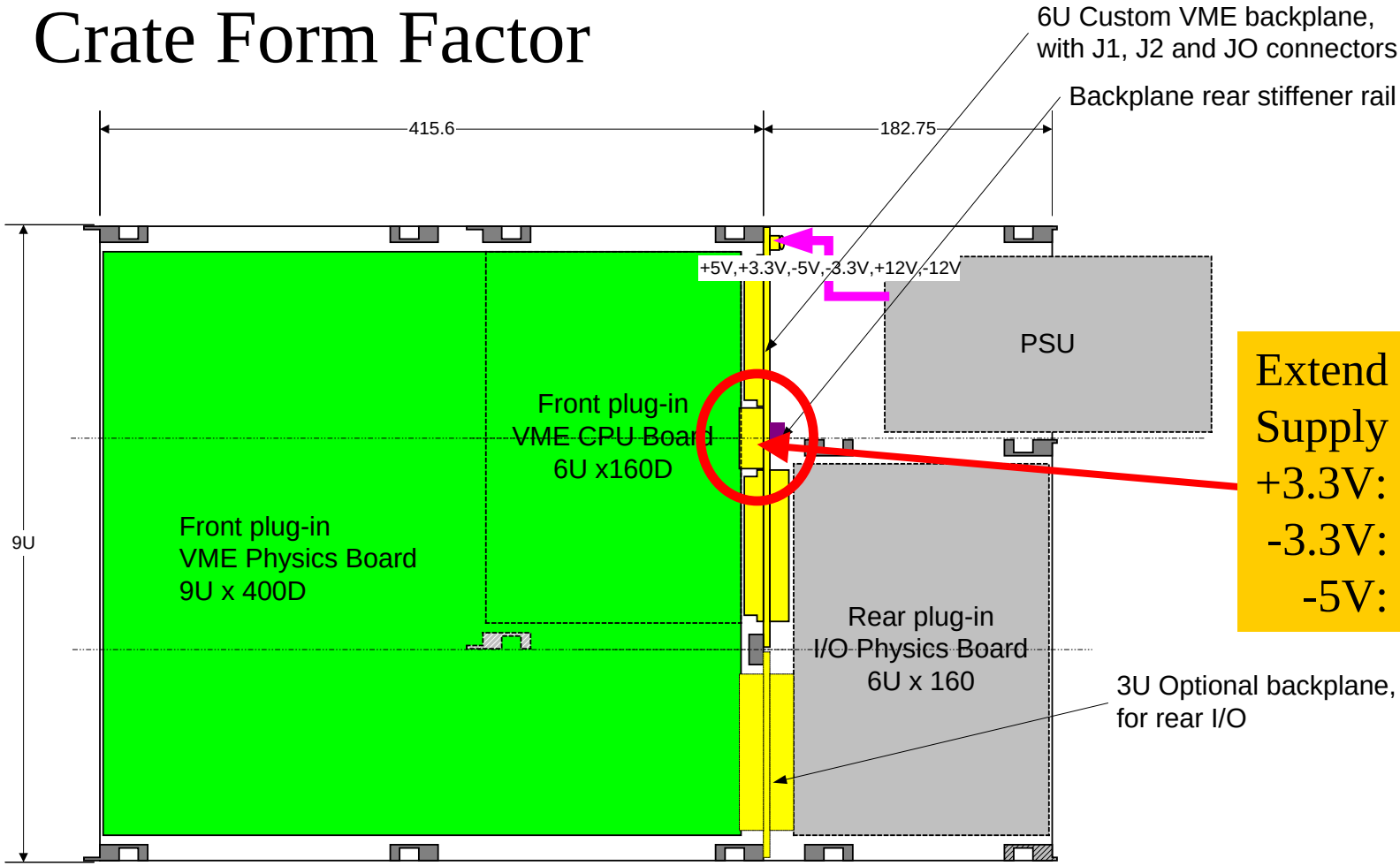
Voltage	-5.0V	-3.3V	+3.3V
Total Max Current	100A	320A	200A

Pos.	z	a	b	c	d	e	f
1	GND	GND	GND	GND	GND	GND	GND
2	GND	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND
4	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
5	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
6	GND	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
7	GND	+3.3V	+3.3V	GND	GND	GND	GND
8	GND	GND	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	-3.3V	-3.3V	GND
11	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
12	GND	-3.3V	-3.3V	-3.3V	-3.3V	-3.3V	GND
13	GND	GND	GND	GND	GND	GND	GND
14	GND	-5V	-5V	-5V	-5V	-5V	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	S1+	S1-	GND	S2+	S2-	GND
17	GND	S3+	S3-	GND	S4+	S4-	GND
18	GND	S5+	S5-	GND	S6+	S6-	GND
19	GND	S7+	S7-	GND	C1	C2	GND

Pin assignment of power supply connector (IEC 61076-4-101)



Crate Form Factor



Extend Power Supply Connector
+3.3V: 320A
-3.3V: 200A
-5V: 100A

VME 9U base

Side View

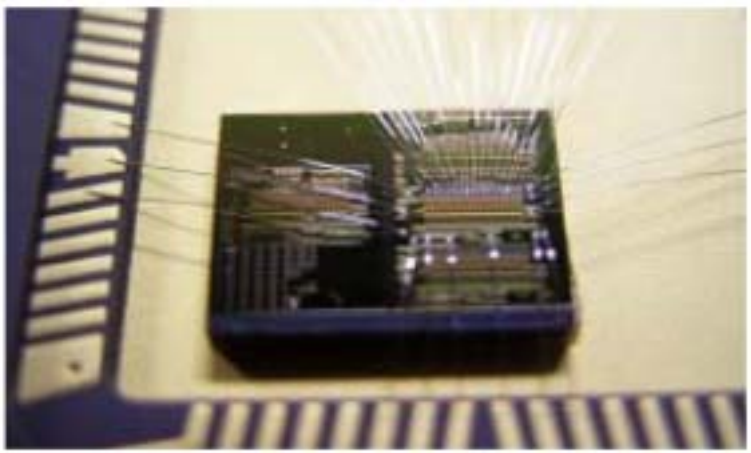
KEK 9U Custom VME Subrack Plan - Rev. 0.1 for High Energy Physics Experimentation
(Shimada Aug.13,2002)

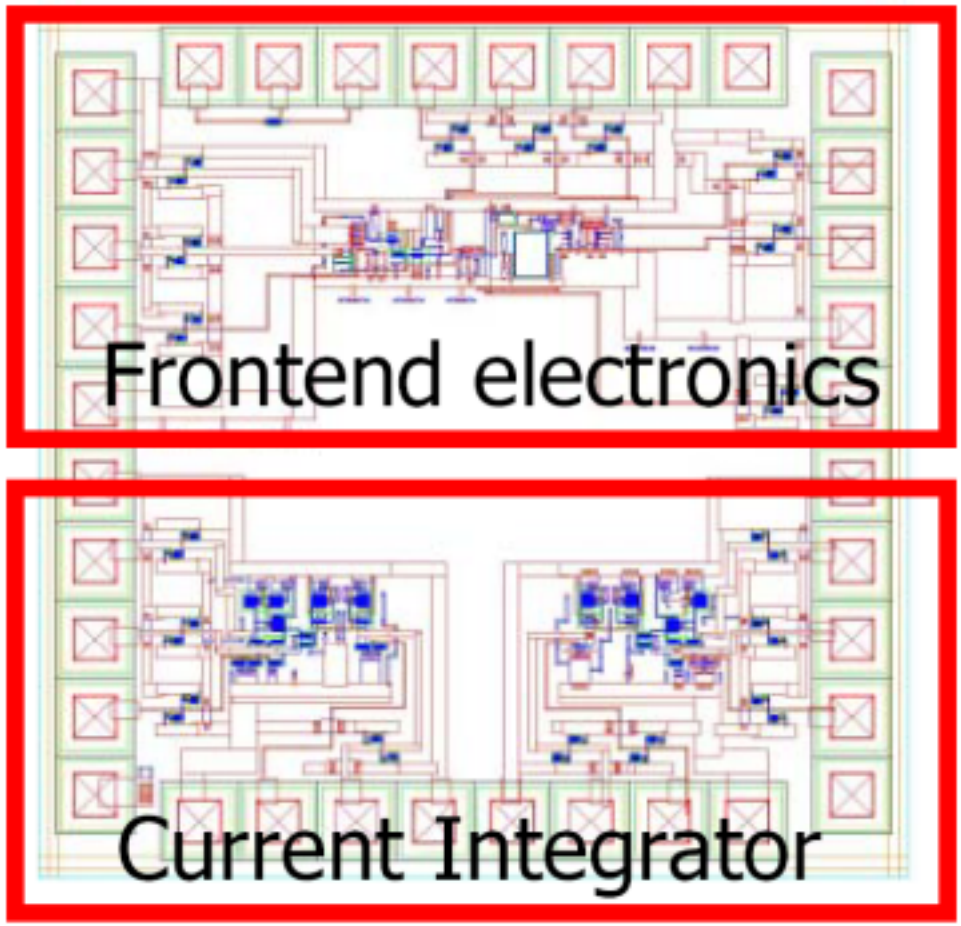
KEK-VME crate and Read-out modules

COPPER/FINESSE(jig)/EPC-6315/PMC-memory

ASIC Current Integrator

- Bipolar 0.6μm
- ft : 2~20 GHz

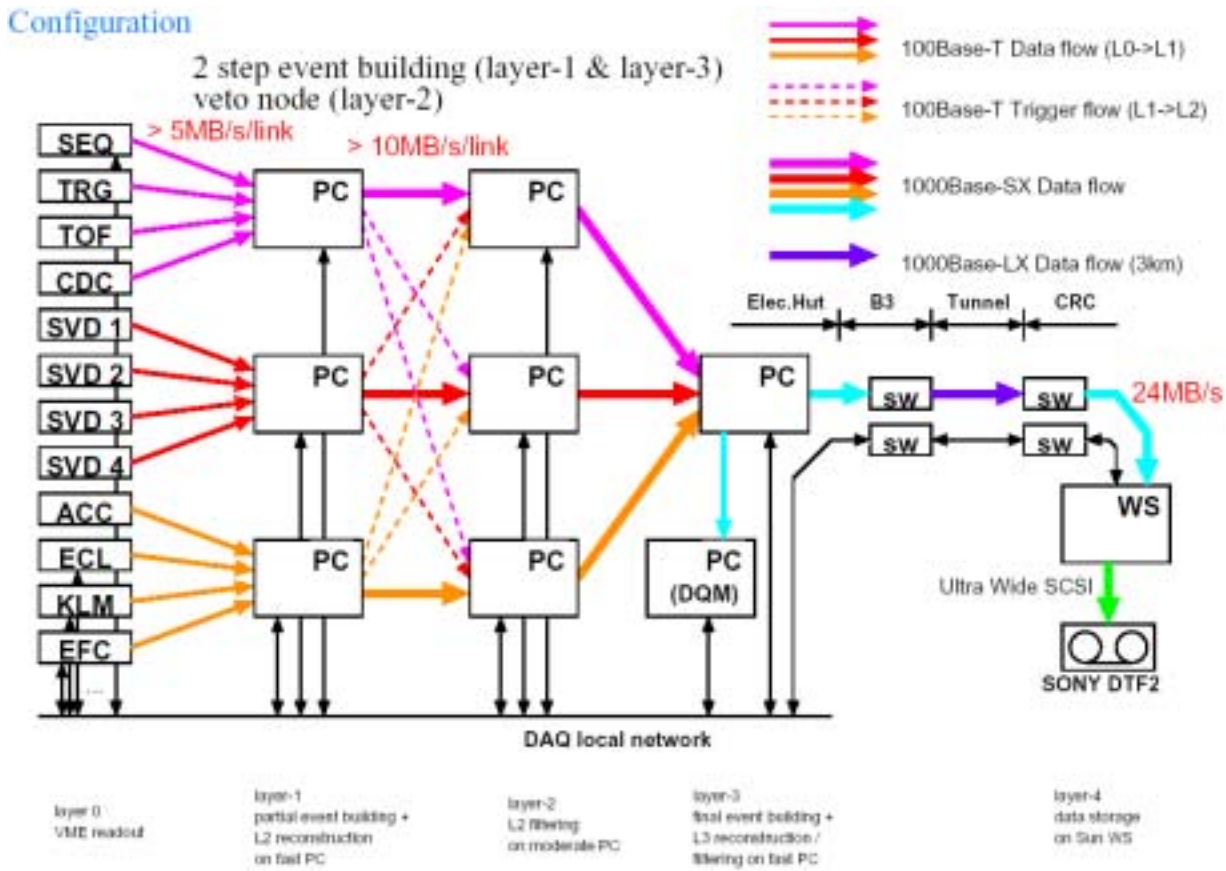




KEK electronics group

Event Builder

- Ethernet base event builder is works well under ~10 MB/sec data flow condition.
- We expect this system works well under ~50MB/sec data flow condition by the layer tuning.



Belle Network Event Builder Configuration