

# DAQ system at the Engineering Run on 2002 for KEK PS-E391a experiment

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## **Abstract**

This document describes the data acquisition system for the KEK PS-E391a experiment. The hardware and the software components used in the engineering run in autumn 2002 are explained in detail.

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# 1 Introduction

The engineering run with a part of the E391a detector was carried out in autumn 2002. Since we have only one chance of physics run on 2004 in the present schedule of the KEK-PS operation, the engineering run is crucially important for the success of the experiment. We have done the overall check of our experimental apparatus including the electronics and data acquisition system, as well as the precise calibration of each detector.

## 2 E391a detector

Figure 1 shows the schematic view of the E391a detector. It composed of the electromagnetic calorimeter and hermetic veto system. Events accompanying with charged particles are rejected by the scintillation counters in front of the CsI. The veto system for additional particles, which consists of the central-barrel calorimeter, front-barrel calorimeter, beam-anti counter and five-stage of the beam-collar counters, are designed to cover whole decay region without any dead-region. The veto calorimeters consist of the alternating scintillator and lead or tungsten plate with wave-length-shifter fiber read-out. The total number of channel is about 900, which includes 576 for CsI array, 32 for the front-barrel calorimeter 192 for the central-barrel calorimeter, 22 for the series of beam-collar calorimeters, 32 for the charged-veto scintillation counters and 40 for the beam-anti detector.

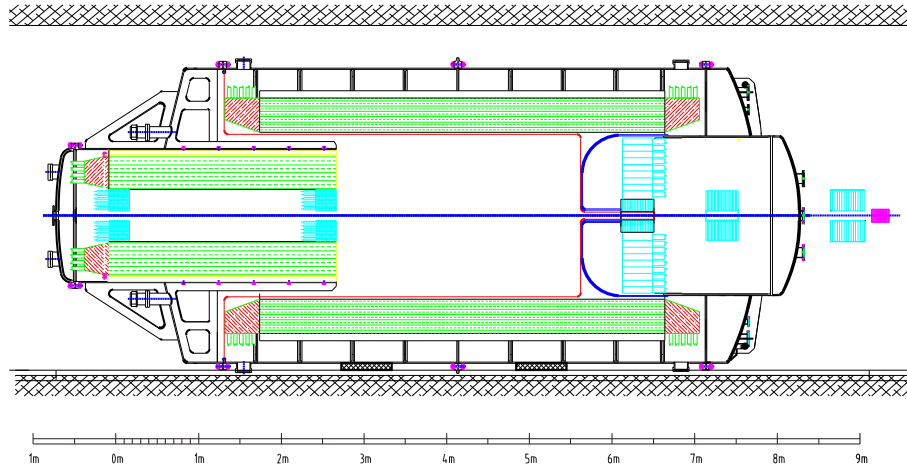


Figure 1: E391a detector.

As of autumn 2002, the downstream section containing the CsI active detector, small sandwich calorimeter located at the CsI-supporting cylinder-edge, charged-veto scintillation counter and one of the beam-collar counter at the center of CsI array, were fabricated and used for the engineering run.

## 3 DAQ system

### 3.1 Requirement

Requirement for our DAQ system is summarized in the Table 1.

Number of detector channels	900
Number of ADC channels	1200
Number of TDC channels	1000
Number of multihit TDC channels	100
Energy measurement	1 MeV to 3 GeV
Energy resolution	50 fC
Timing measurement	200 nsec for full scale
Timing resolution	< 50 psec
Multihit timing measurement	up to 2 $\mu$ sec
Data size of ADC	1200 $\times$ 4 byte /event
Data size of TDC	< 200 $\times$ 4 byte/event
Data size of multihit TDC	< 400 $\times$ 4 byte /event
Data size	3 Mbyte/spill
Trigger rate	200 Hz (500 Hz for physics run?)
Data transfer speed	>20 Mbyte/sec

Table 1: Requirement for our DAQ system.

### 3.2 Overview

Figure 2 shows the overview of the DAQ system. The network distributed system with multiple CPU was employed for the flexibility and scalability for future upgrades. The parallel-processing frontends contribute to reduce the total dead-time. Data from each frontend are collected by the data collection server. The collected data is at first written on the local disk on the collection server, then send to the large tape-library system at the KEK central computing facility. A local DLT drive is attached to the data collection server in case of the emergency such as the trouble on the network between the data collection server to the large tape-library.

## 4 Electronics

### 4.1 ADC system

#### 4.1.1 ADC module

In order to measure the 1 MeV energy precisely, the ADC resolution of 10 channel per 1 MeV will be preferable. This correspond to 50 fC per channel of resolution when we assume the 1 mV of pulse height delivered by the 50  $\Omega$  impedance cable. We should also measure the  $\gamma$  energy up to 3 GeV for the higher energy  $K_L$ . Thus the dynamic range of ADC is required to be from 50 fC to 1500 pC. The LeCroy 1885N 96ch FASTBUS ADC, which was used in the VENUS and TOPAZ experiment

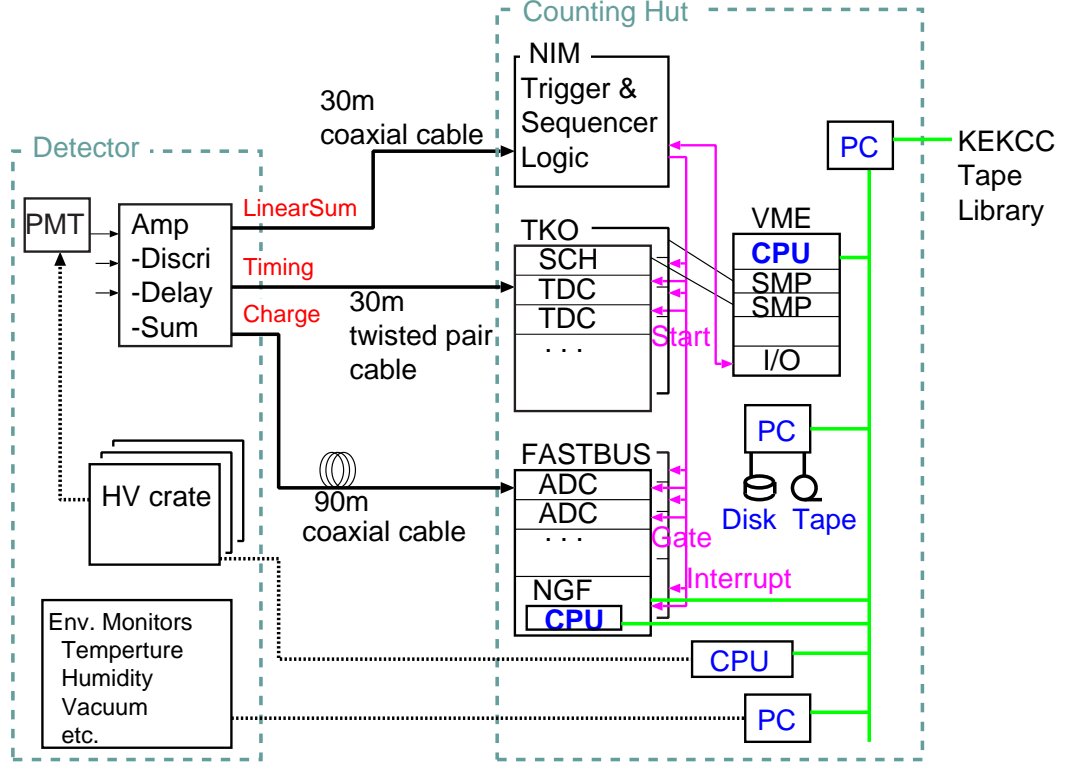


Figure 2: DAQ system overview.

at KEK TRISTAN accelerator, satisfies this specification. We could make use of enough channels of this ADC as a recycle from the stock room, which also lead to the significant cost reduction. The deficit of this ADC is that the data conversion time is so long ( $750 \mu\text{sec}$  in the specification sheet), and the block-transfer mode is not available for the read-out, and also it does not have the pedestal-suppression capability in hardware. These restriction limits the data acquisition speed up to 1000 Hz at most.

#### 4.1.2 FASTBUS controller

The SIS4100 NGF (Next Generation FASTBUS) is used as the FASTBUS-to-VME interface. It has the FIFO memory of 4 kbyte depth as the read-out data buffer. It also has the capability of DMA transfer from FASTBUS to VME memory in order to support the block-transfer mode of the FASTBUS read-out cycle. The sequencer and the command-list processing system of NGF can make the readout from ADCs easier and faster.

The control of the NGF is done by the VME FORCE54 UltraSPARCII 500 MHz CPU board. The operating system of Sun Solaris8 is chosen since the VME driver for the Solaris8 is officially supported by the CPU vender of FORCE-computer-system, and the KEK online group also support some useful tools such as CAMAC driver for this combination.

We use two sets of the FASTBUS-NGF system to read the total of about 1200 channels of the detector signals. Each set includes six ADCs, one NGF and one

logical-addressing-board in the FASTBUS slot. Total of 576 channels are read in a triggered event and stored into the FIFO buffer of NGF. The data size for one channel is four bytes, thus the FIFO buffer can hold no more than one event at a time.

#### 4.1.3 Trigger-event sequence

The read-out sequence of one trigger event is as follows. In the initialization of NGF, the command list to read one event is written into the command-list memory of NGF. When the global trigger signal is generated at the global trigger decision system, it generates the signal to start the ADC readout after waiting for 750  $\mu$ sec for the ADC conversion. This signal is fed into the sequencer-start input of the NGF, then the NGF loads the command-list from the command-list memory and execute them. The NGF start reading the ADC channels one by one and store them into the FIFO according to the command list. After finishing the command list to read all channels, the NGF generates the logic signal and fed it into the input channel of the VME I/O register module. When the CPU detect the input signal of the I/O register by polling, it starts the data transfer from FIFO of NGF to CPU memory. After this transfer is done, the CPU generates the logic signal and send it as the sequence-finished signal to the global trigger decision system. The global trigger decision system clears the trigger-veto latch by this signal, and start waiting for the next event trigger.

### 4.2 TDC system

#### 4.2.1 TDC module

In order to reduce the accidental background events, 1 nsec of the event-timing resolution will be required. In some cases, we also have to distinguish the incident angle of  $\gamma$  to the CsI crystal array for the further reduction of the background. For that purpose, less than 0.1 nsec of the timing resolution will be necessary. Fortunately, the KEK electronics facility already developed such a high-resolution TDC circuit. For our experiment, we decided to use 64ch TKO-TDC (TKO : TRISTAN-KEK-Online standard system) as a TDC module, since we already had the 16ch TKO-TDC module and it was easy to create a high-density TDC module by simply extend this modules by factor of four. The TDC is operated in the common-start mode only.

#### 4.2.2 TKO controller

TKO system is a simple system for the module operation. It is controlled by the intelligent TKO interface, SCH (Super Control Header), connected with with the VME dual-port memory module, SMP (Super Memory Partner). The SCH can be controlled through the SMP command register by the VME FORCE54 Ultra-SPARCII 400 MHz CPU board. Since the SCH has the programmable hardware data-suppression function, it can accumulate more than 1000 event of data of the E391a detector channels into the SMP memory that has one Mega-word of the data buffer size.

### 4.2.3 Trigger-event sequence

The readout sequence is completely done by the hardware signal of SMP and SCH. In the initialization of SCH, the CPU selects the readout mode of the SCH and set the data suppression database. When the global trigger signal is generated at the global trigger decision system, it waits for 100  $\mu$ sec which is the conversion time of the TDC module, and generates the signal to start the TDC read-out. This signal is fed into the event-accept input of the SMP, then the SMP send the sequencer-start command to the SCH. The SCH read the data with suppressing the unnecessary data by the selected sequence, and transfer the data to SMP memory in certain format. The event-sequence-finished signal to the global-decision-system is generated by using the complement of the busy signal of SMP. The buffer-change of the SMP memory port can also be done by a hardware signal from the global trigger decision system. The CPU does not have to do anything about this event read-out sequence. Only the CPU has to do is to read the whole data in the SMP memory after the buffer is changed. The buffer-change is noticed to CPU by the interrupt signal from the SMP. Since the SMP has the dual-port memory, it can accept the data writing from SCH to one buffer even during the data reading for another buffer by the CPU. This way we can reduce the dead-time the event processing quite small.

## 4.3 Multihit TDC system

### 4.3.1 TDC module

Multihit TDC is useful in some cases. We might want to measure the longer time scale than the TKO-TDC for the study of the trigger, background or accidental hits. We also might want to observe the pile-up of the calorimeter hits by a multiple gammas.

We have chosen the LeCroy 1877S FASTBUS TDC for those measurements. It has 96 channels in a module, and each channel has the 16 depth of the buffer. The dynamic range is 16 bit for the full scale of 32  $\mu$ sec. Thus the resolution is 0.5 nsec, which would be enough for those purpose. The data conversion time is less than 80  $\mu$ sec on the specification sheet. The block transfer is available for this TDC. We used one TDC module in the engineering run.

### 4.3.2 Control

Since the 1877S TDC was installed in the same FASTBUS crate as the 1885N ADC, it was controlled and read by the NGF system. The trigger-event sequence is the same as that for the 1885N ADC except for the common-stop timing. By using the block-transfer mode, the dead time for reading the data from one 1877S TDC was about 30 msec, which was quite small compared to that for the 1885N ADC, and that it affects little to the total dead-time of DAQ.

## 4.4 Scaler

We have chosen the CAMAC 12ch 24bit scaler to count the various kind of numbers. They are read once in a spill just after the spill-end by the same VME CPU



as controls the TKO-TDC through a VME-to-CAMAC interface, Kinetic systems K2917 and K3922. 10 modules are used in the engineering run in 2002.

We also used the VME visual scaler which has the VIDEO output so that the experimental shifter can see the number of each counters on the TV screen. Some of the important number to be recorded on the shift report such as the SEC, Target Monitor, N-cluster before and after the trigger-logic, are displayed on screen.

## 4.5 Clustering module

In order to distinguish the small signal of 1 mV, we newly developed the signal discrimination module, so-called the Amp-Discri-Delay-Sum (Amp-Discri) module. This module can produce three kinds of output simultaneously; the analog signal for ADC, timing signal for TDC and analog-sum signal for trigger, so that the cabling in the latter stage of triggering and sequencer logic circuit would become easier. Figure 3 shows the schematic view of the Amp-Discri module. The analog output for the ADC (Through), the delayed logical output for the TDC which is the discriminated signal of amplified analog signal by 36 times, two linear-sum signal and one amplified-sum signal of the 8 channels are shown. The circuit is installed into the NIM-standard frame-box. The threshold of the discriminator for the TDC signal can be adjusted by the trimmer at the front panel.

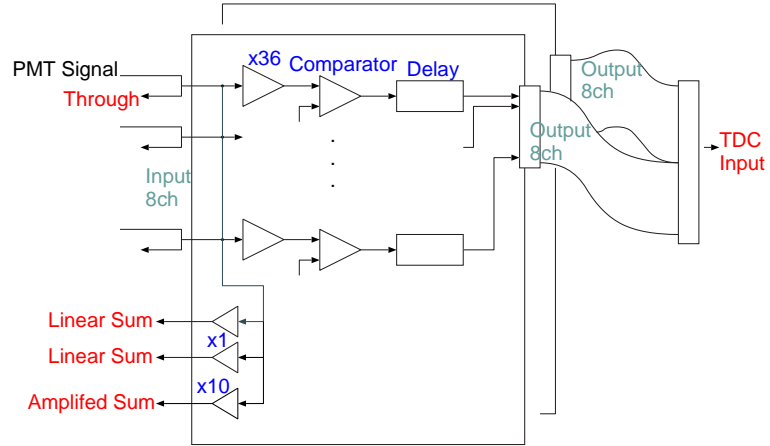


Figure 3: Schematics of Amp-Discri-Delay-Sum module.

Since the detector signal should be processed by the Amp-Discri module as early as possible to avoid the possible noise and the attenuation, the Amp-Discri modules are installed in the NIM bins located just behind the detector.

## 4.6 Trigger and sequencer logic

### 4.6.1 Global Trigger logic

The global trigger logic accepts the multiple trigger signal simultaneously from the multiple subsystem. For example in the engineering run from October to December 2002, the random trigger from the clock generator, cosmic-ray event from cosmic

counter, xenon-flash trigger for the gain monitoring system of PMTs, radioactive-source trigger for the another gain monitor, and the number-of-CsI-cluster trigger (N-cluster) from the cluster-counting logic, are used as the multiple trigger input. The global trigger logic is made of the combination of the NIM modules to produce the event-trigger signal within 200 nsec after the trigger-request from the subsystem. Only this level of the trigger is used for the trigger decision, and no further reduction of the trigger rate is done in the current scheme of the system. The total trigger rate in the engineering run in 2002 was about 200 Hz when we required  $N \geq 6$  for the N-cluster trigger, and the dead time was about 30%. Figure 4 shows the block diagram of the global trigger logic used in the engineering run in 2002. The information of which subsystem issued the trigger-request can be obtained by the trigger-bit pattern output. They are fed into the input channels of the VME I/O module in the NGF and recorded by the CPU.

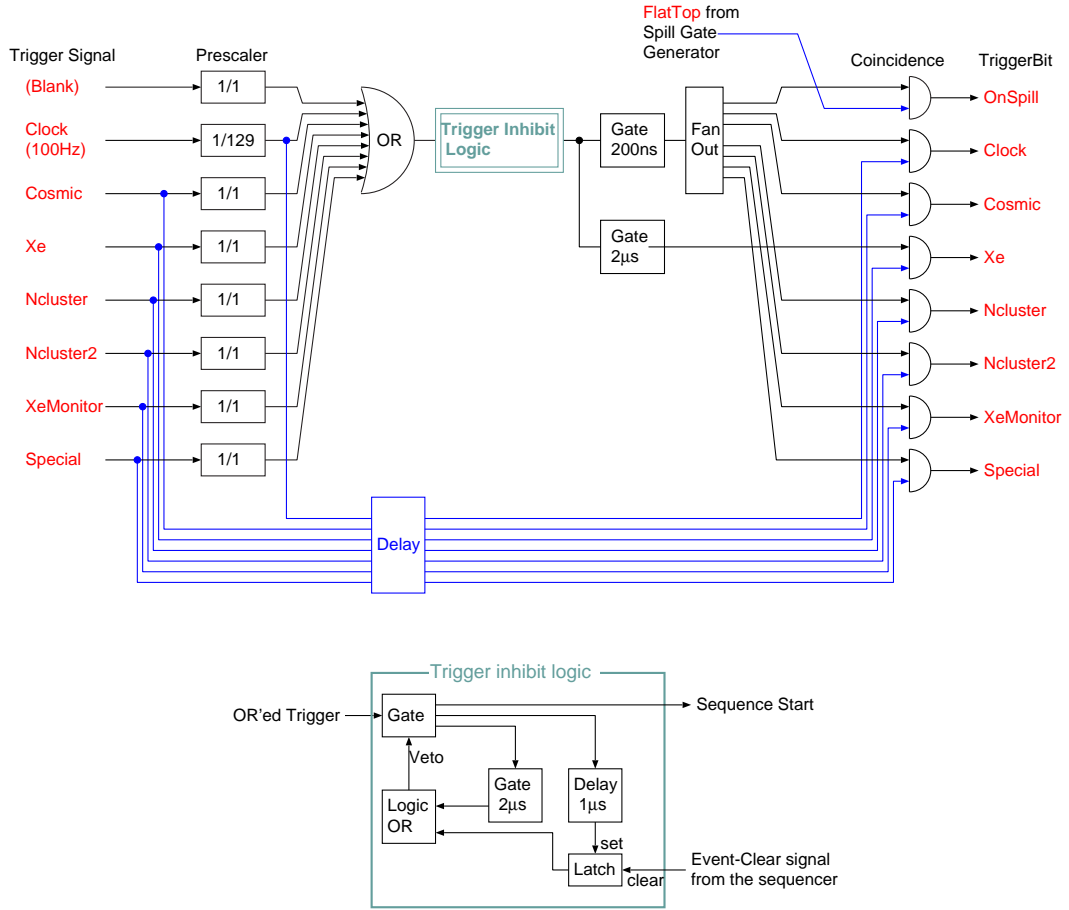


Figure 4: Block diagram of the global trigger logic.

#### 4.6.2 N-cluster trigger

Figure 5 shows the block diagram of the N-cluster trigger for the CsI cluster counting. Linear-sum signals from the Amp-Discriminator module are discriminated at the certain pulse height and fed into the multiplicity-logic module. Total of 72 linear-sum

signals are fed into the five multiplicity-logic modules.

### Ncluster Trigger

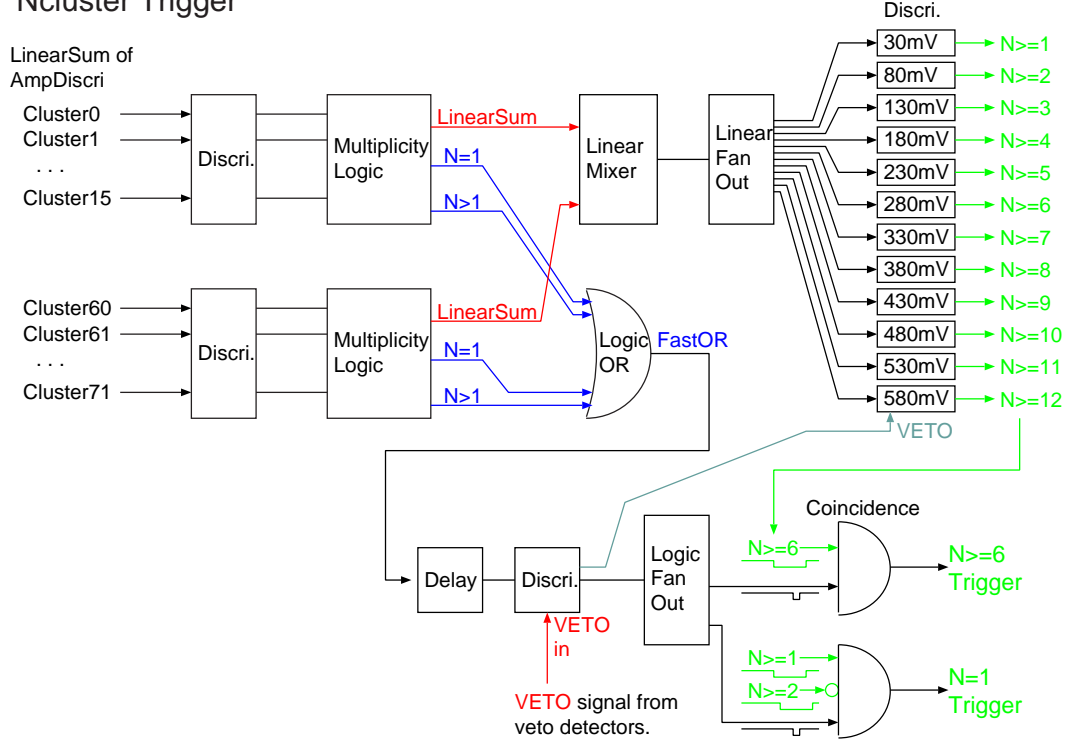


Figure 5: Block diagram of the N-cluster trigger logic for CsI cluster counting.

### Veto signal

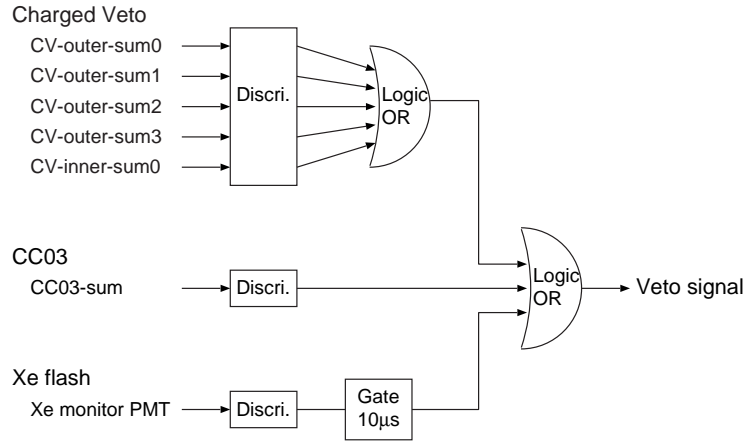


Figure 6: Block diagram of the trigger-veto logic for Veto detectors.

The multiplicity-logic module produces the level-signal from the linear-sum output whose height is proportional to the number of hits in the module. It also produces the logic-signal from the  $N = X$  output when the number of hits in the module is exactly equal to the  $X$ , and from the  $N > X$  when the number of hits is

greater than  $X$ . The number  $X$  can be changed from 1 to 8. The linear-sum output of the multiplicity-logic modules are fed into the linear-mixer module to measure the total number of hits in the CsI cluster by the summed pulse-height. Since one hit corresponds to the 50 mV of pulse height, we can count the total number of hits by using the multiple discriminator in a different discrimination level which is apart from 50 mV each other.

The trigger-timing for the  $N$ -cluster trigger is determined by the earliest hit in the CsI cluster. This is realized by using the OR of the logic-outputs of the multiplicity-logic module (Fast-OR). The signal from  $N \geq X$  discriminator comes earlier into the coincidence module. The signal from the Fast-OR is adjusted to come later into the coincidence module by a certain delay. Thus the output timing of the coincidence module is always defined by the Fast-OR signal. The discriminator for the  $N \geq X$  is vetoed by the delayed Fast-OR signal so that they would not produce the signal later than the Fast-OR signal. The veto signal from the veto-detectors such as the collar-counters or charged-veto counters are used to kill the Fast-OR signal before the coincidence module, as shown in Figure 5 and 6.

#### 4.6.3 Cosmic trigger

We have six long scintillation counters for the cosmic trigger. Four are located above the CsI cylinder, and two are below. The coincidence of the OR of the signal of four counters above and OR of the signal of two counters below are used for the cosmic trigger signal.

#### 4.6.4 Xe flash trigger

Xe flash lamp is used for our system to monitor the gain of the PMT. The light is distributed by the optical fiber not only to all CsI crystals but also to the seven reference PMT. One of the reference PMT is used as the Xe flash trigger. The frequency of the Xe flash is controlled by the clock generator and the prescaler. In the engineering run in 2002, we used 1/3.3 Hz of the frequency for the physics run.

#### 4.6.5 Reference PMT monitor

We have another system to monitor the gain of the reference PMT. The  $^{241}\text{Am}$  is attached to the face of the six reference PMT. The OR of the six reference PMT signal is used for the reference PMT monitor trigger. The OR'ed signal rate is roughly 100 Hz, and is prescaled by 1/600.

#### 4.6.6 Random trigger

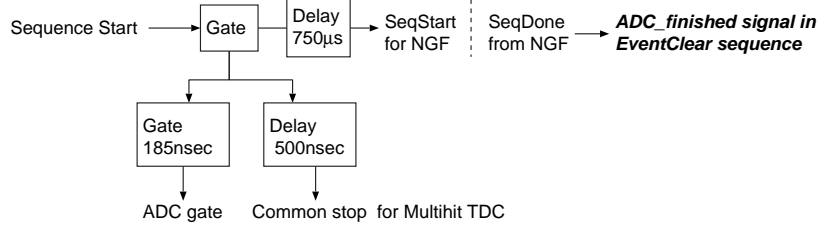
Random trigger is generated by clock generator module, and prescaled to 1/1.29 Hz.

#### 4.6.7 Global Sequencer Logic

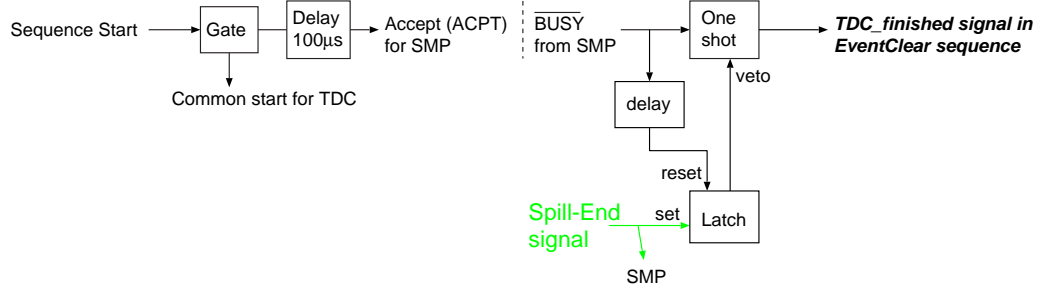
The sequencer logic for the operation of ADC and TDC is shown in Figure 7 and 8. It consists of the DAQ-start sequence, read-out sequence, event-clear sequence and buffer-change sequence.

## Event Sequence

### ADC and Multihit\_TDC sequence



### TDC sequence



### EventClear sequence

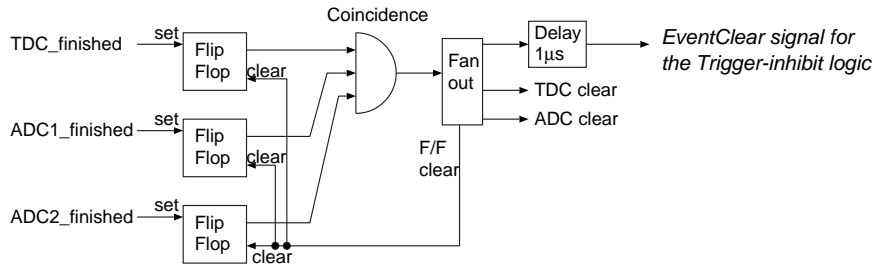


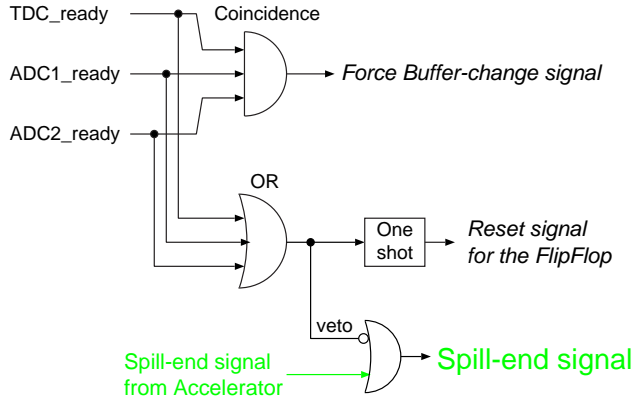
Figure 7: Block diagram of read-out and event-clear sequence logic.

The DAQ-start sequence is the special sequence only issued at the beginning of each run to synchronize the multiple frontends. It clears all the flip-flop, wait for all the DAQ frontend to be ready, then issue the buffer-change sequence. The buffer of each frontend is then cleared, and they are ready to accept the trigger event.

The read-out sequence in the global sequencer logic wait for data conversion of ADC and TDC for a certain time after the global sequence started, then issue the signal for each frontends to start its actual read-out sequence from the ADC and TDC modules.

The signal to notify that the frontend finished its read-out sequence is generated by the CPU through the NGF for the FASTBUS ADC, and by the SMP BUSY signal for TKO TDC. The sequence-finished signal in the TDC event sequence is produced somehow complicated logic so that the BUSY signal during the buffer-change sequence does not produce the fake sequence-finished signal. The event-clear signal is generated by the coincidence of these sequence-finished signals. It is fed into the fast-clear input of ADCs and TDCs. It also fed into the trigger-inhibit

### DAQ-start sequence



### Buffer-change sequence

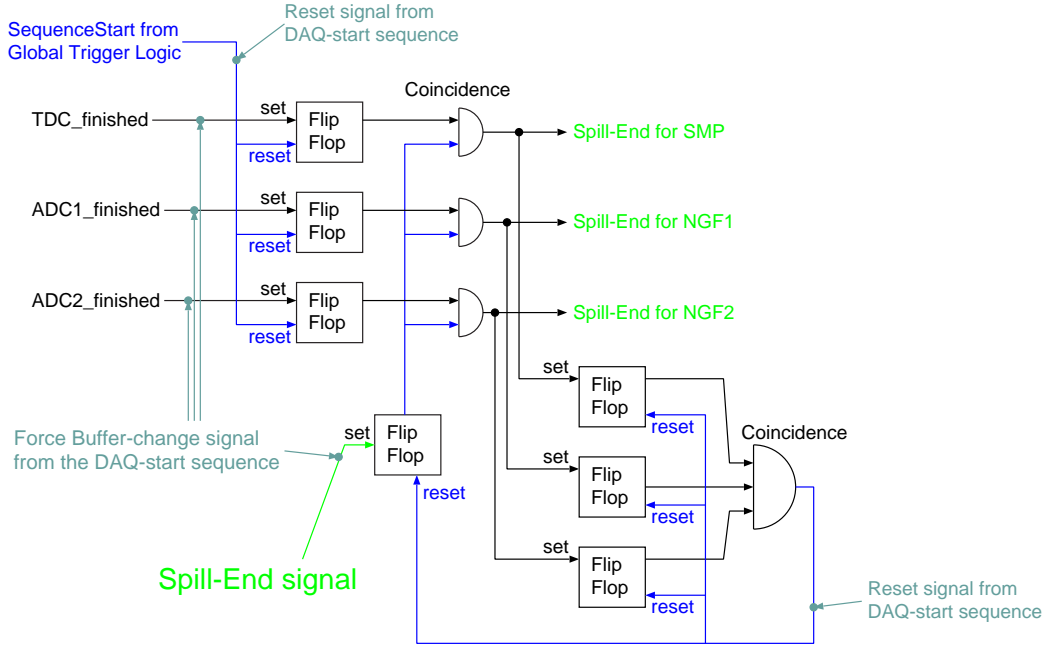


Figure 8: Block diagram of DAQ-start and buffer-change sequence logic.

after waiting for the completion of the fast-clear command for ADCs and TDCs for 1  $\mu$ sec.

The buffer-change sequence is issued at each spill-end. If the spill-end signal is issued when the event-sequence is not active, then the buffer-change signal is immediately fed into the NGF and SMP. Otherwise, it waits for the completion of the event-sequence for each frontend, then issues the buffer-change signal to them. It is very rare, but might happen, that the spill-end signal is issued just before the event-sequence starts, and that some of the frontends begin their event-sequence but others do not. In this case, that event will be recorded in the data-buffer before the buffer-change for the frontends who began the event-sequence, but will be recorded

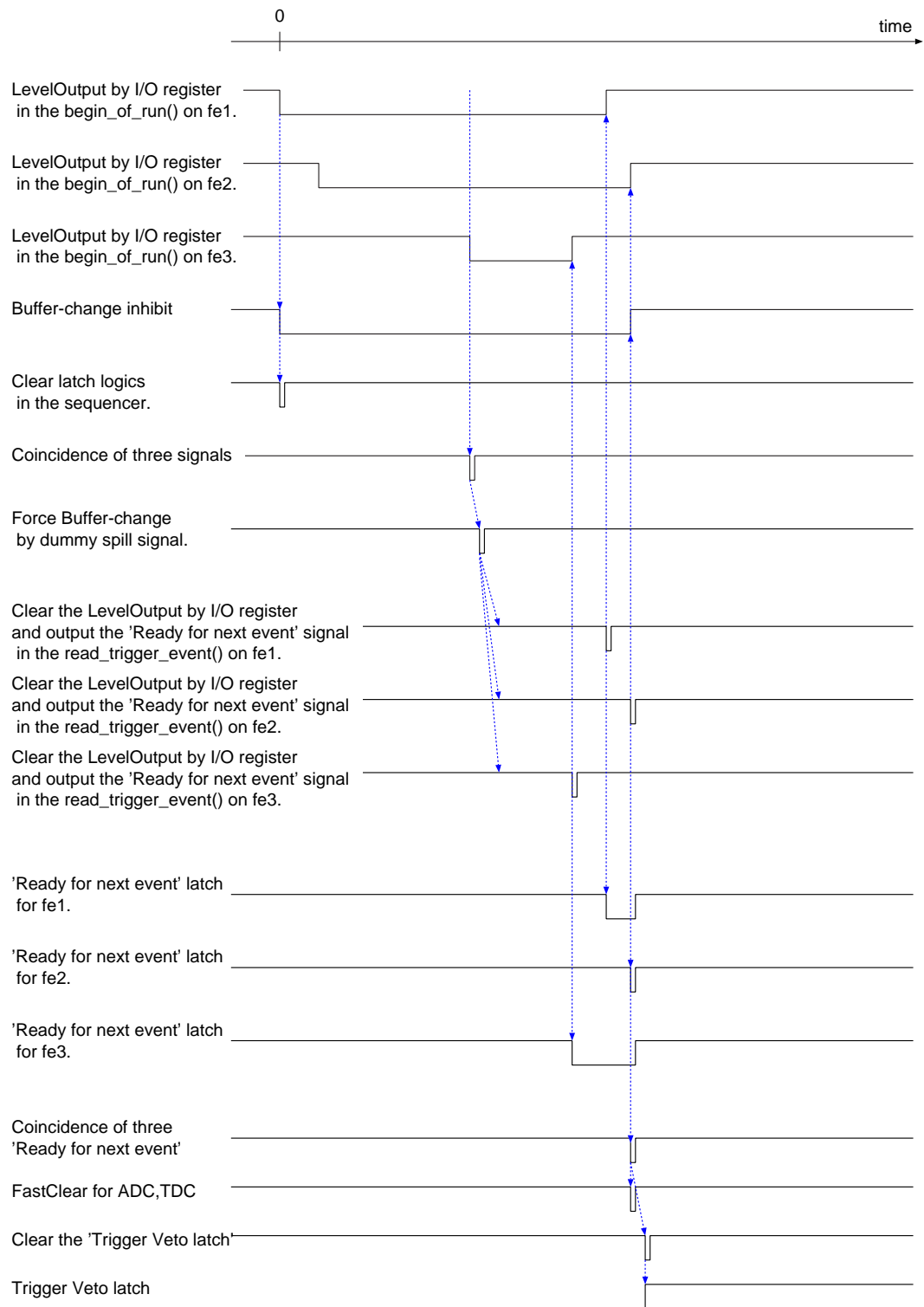


Figure 9: Timig chart for DAQ-start sequence.

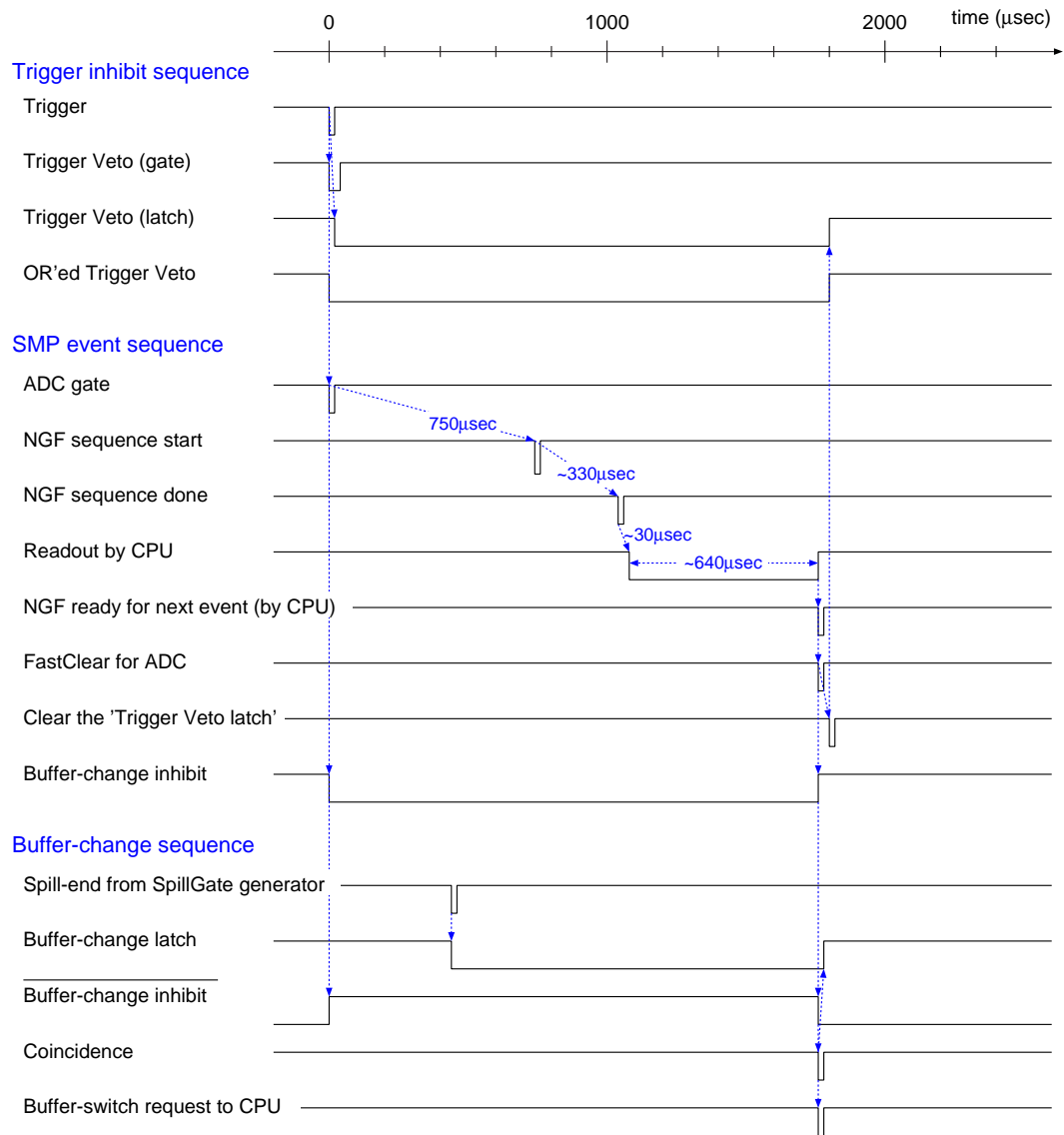


Figure 10: Timig chart for NGF-ADC read-out sequence.



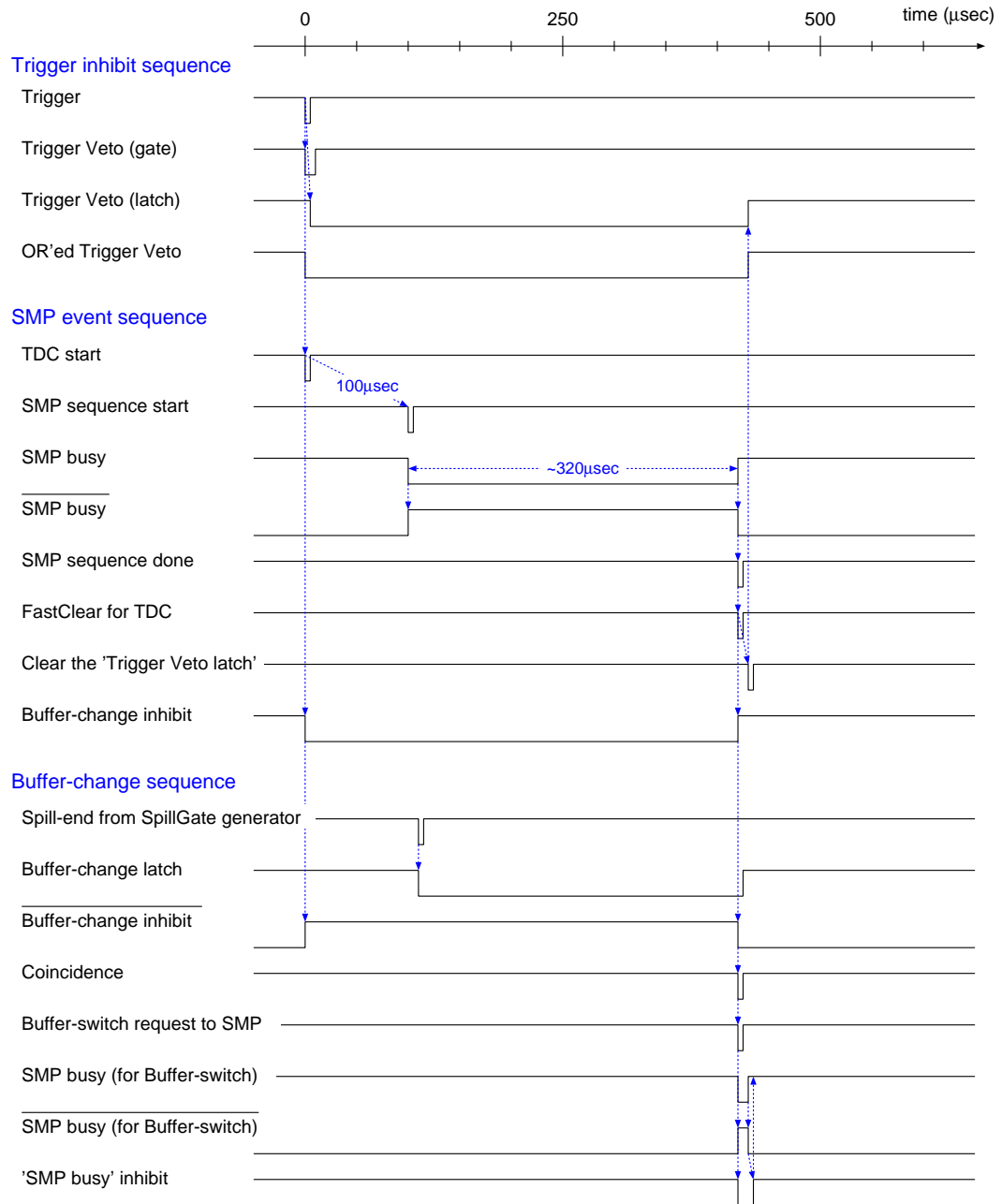


Figure 11: Timig chart for TKO-SMO-TDC read-out sequence.

in the next data-buffer for the frontends who did not begin the event-sequence. This causes the so-called 'event-slip' in the data-buffer. This might not be avoidable in the current scheme, since the control cable between the sequencer and the NGF or SMP has finite length, and that the latency of the signal with these cables will lead to such a timing problem. In the engineering run in 2002, the event-slip problem happened only a few times a day.

A rough timing chart of the DAQ-start, NGF-ADC readout, TKO-SMP-TDC readout and buffer-change, are shown in Figure 9, 10 and 11.

#### 4.6.8 Control-signal cable connection to the NGF and SMP

Figure 12 shows the configuration of the cable connection for the control-signal to the NGF and SMP for your reference.

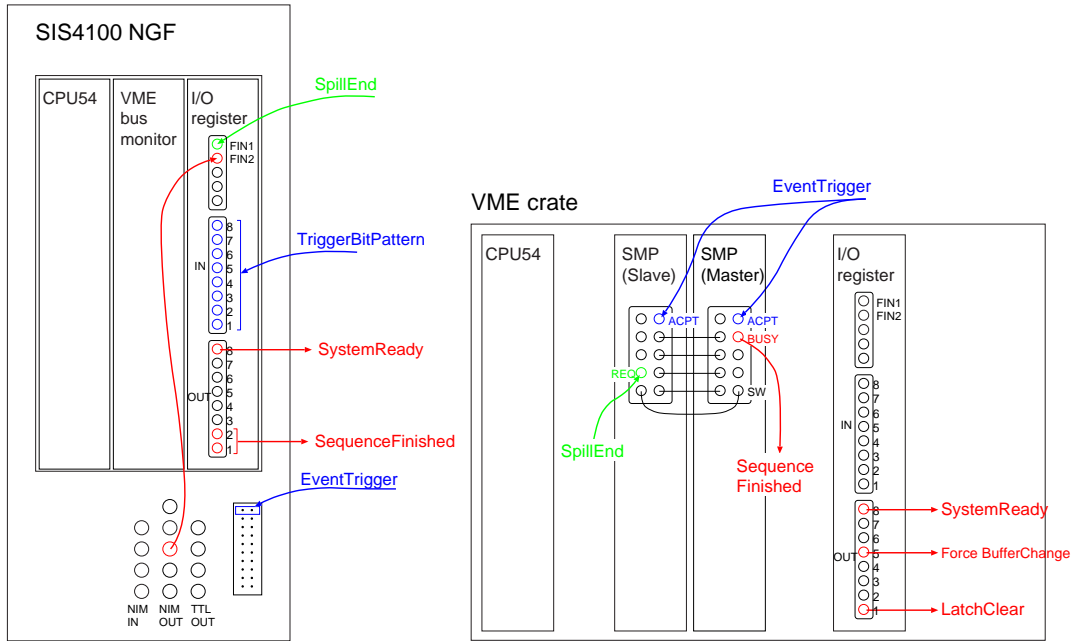


Figure 12: Control-line configuration for the NGF and SMP.

#### 4.6.9 Layout of the NIM and VME modules

Figure 13 shows the layout of the NIM, VME and CAMAC modules in the 19-inch rack used in the engineering run in 2002.

### 4.7 High voltage system

High voltage for the detector PMT is provided by the CAEN A734 negative module installed in the CAEN SY527 crate. One module has 16 channels, and one crate hold up to 10 modules. Thus we need at least 6 crates in total to provide 900 of the detector channel.

The SY527 crate can be controlled either via RS232C serial line or via the special network, CAENET, with the special controller module. We decided to use the

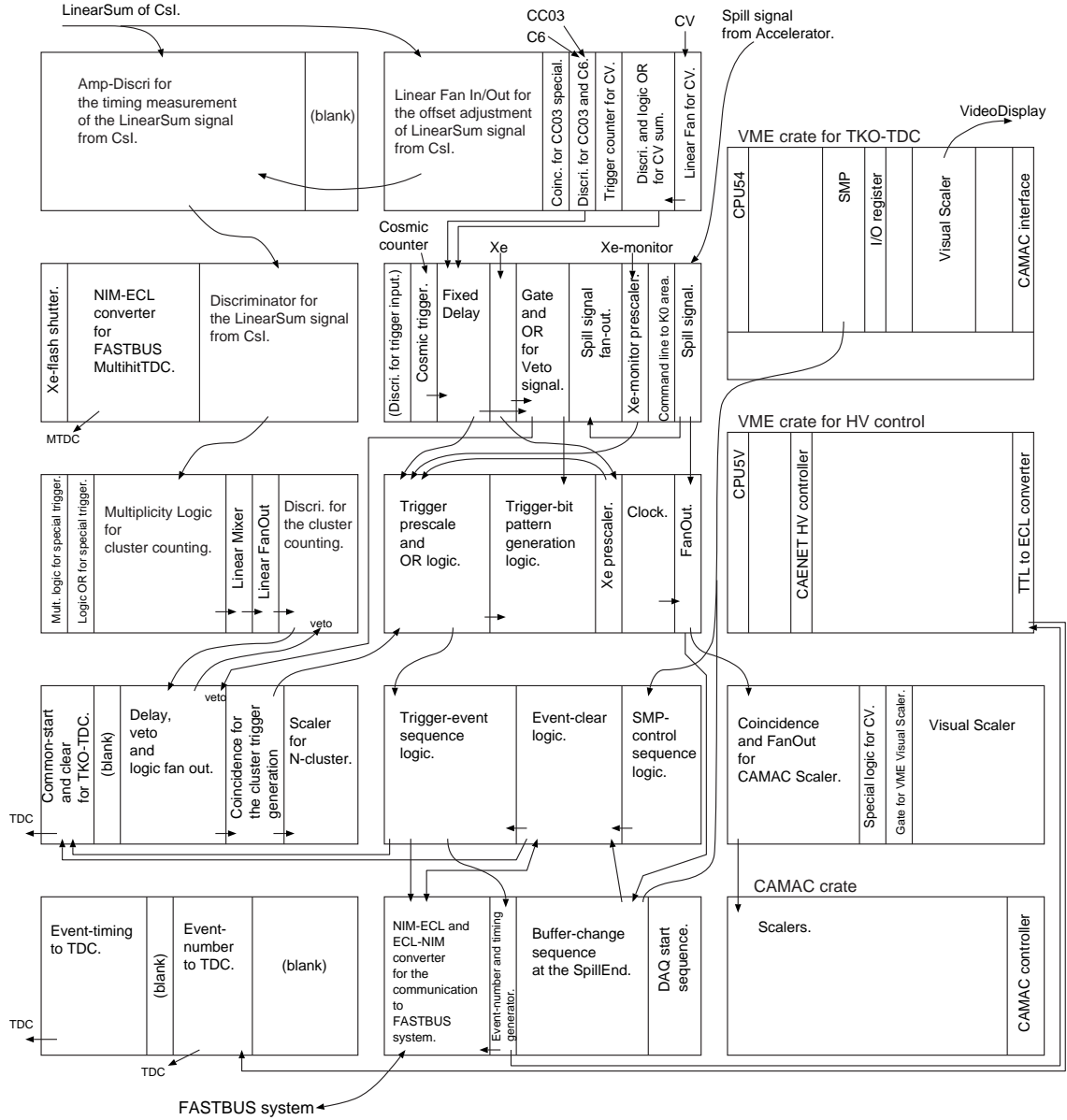


Figure 13: The layout of the NIM,VME and CAMAC modules in the engineering run in 2002.

CAENET since it is more convenient than the RS232C to handle many channels like our detector. The multiple crates can be controlled by a single controller by connecting daisy-chain each other. We use the VME V288 CAENET controller controlled by the FORCE SPARC5V UltraSparc CPU with Solaris8 operating system. In the engineering run in 2002, we successfully operated more than 700 channels with five crates without any serious trouble.

## 4.8 Environment monitoring system

We will measure the environmental status such as the temperature, humidity and vacuum pressure in the detector, and the stability of the electronics modules including the electricity. In the engineering run in 2002, we measured the temperature of several point on the CsI crystal and the PMT, the humidity of the CsI cylinder, and the DC voltage-stability of the NIM bin for the Amp-Discriminator modules and the DC voltage of the FASTBUS crate. The Keithley 2700 and 2701 multimeters with the 7708 multiplexer module were used for these measurement. The temperature was measured with the thermocouple. The humidity was measured with the Vaisala HMW70 humidity and temperature meter. The DC voltage-stability is directly measured by the 7708 module. The example software which was obtained from the web site of the Keithley instrument company, 'The 2700/2701/2750 Integra Up And Running TestPoint Runtime Software Rev. B01', was used to control the multimeters on the Windows PC.

## 4.9 Cables

The number of signal cables and HV cables are listed in the table 2. The cabling scheme for the charge and timing measurement is shown in Figure 14.

During the engineering run in 2002, we noticed that the signal from the innermost CsI crystals, which has smaller size and that uses different PMT than other CsI, was delayed for about 12 nsec than other CsI. For those CsIs, we replaced the signal feedthrough cable with a shorter one by 12 nsec which directly connects the PMT and Amp-Discriminator clustering module without the feedthrough. In the physics run, these cable should pass by the feedthrough,

The signal cables between the detector and the electronics hut were put on the cable-tray covered with a 1mm-thick iron-plate with copper-foil attached inside the plate. This might play a role of the shield box so that the electrical noise might be reduced to some level. Figure 15 shows the layout of the signal cable-tray.

## 4.10 Ground

The stable and low-impedance ground line is quite important to reduce the noise on the signal cable. We constructed the new ground line under the experimental area. The copper-mesh line covered with the HOKUDEN EP1, which is a electric-conductive concrete, was used. The impedance was measured to be less than 1  $\Omega$ , which is quite good compared to the ordinary ground line.

Downstream	analog	RG58C/U	672	90m	lemo
	analog sum	RG58C/U	80	90m	lemo
	digital	Twist	41	30m	40pin header
	trigger	3D-FB	80	30m	lemo
	feedthrough	RG174U	700	7m	BNC-lemo
	HV	RG174U(?)	634	8m	lemo, SHV
Front	analog	RG58C/U	48	90m	lemo
	analog sum	RG58C/U	6	90m	lemo
	digital	Twist	3	30m	40pin header
	trigger	3D-FB	6	30m	lemo
	feedthrough	RG174U	??	10m	BNC-lemo
	HV	RG174U(?)	48	10m	SHV
Middle	analog	RG58C/U	192	90m	lemo
	analog sum	RG58C/U	24	90m	lemo
	digital	Twist	12	30m	40pin header
	trigger	3D-FB	24	30m	lemo
	feedthrough	RG174U	??	10m	BNC-lemo
	HV	RG174U(?)	192	10m	SHV
PatchPanel	analog	RG174U	1152	2m	lemo-lemo(panel)
	analog	RG174U	1152	2m	lemo-36pin header

Table 2: List of the cables necessary for E391a detector.

Cabling for Charge and Timing measurement

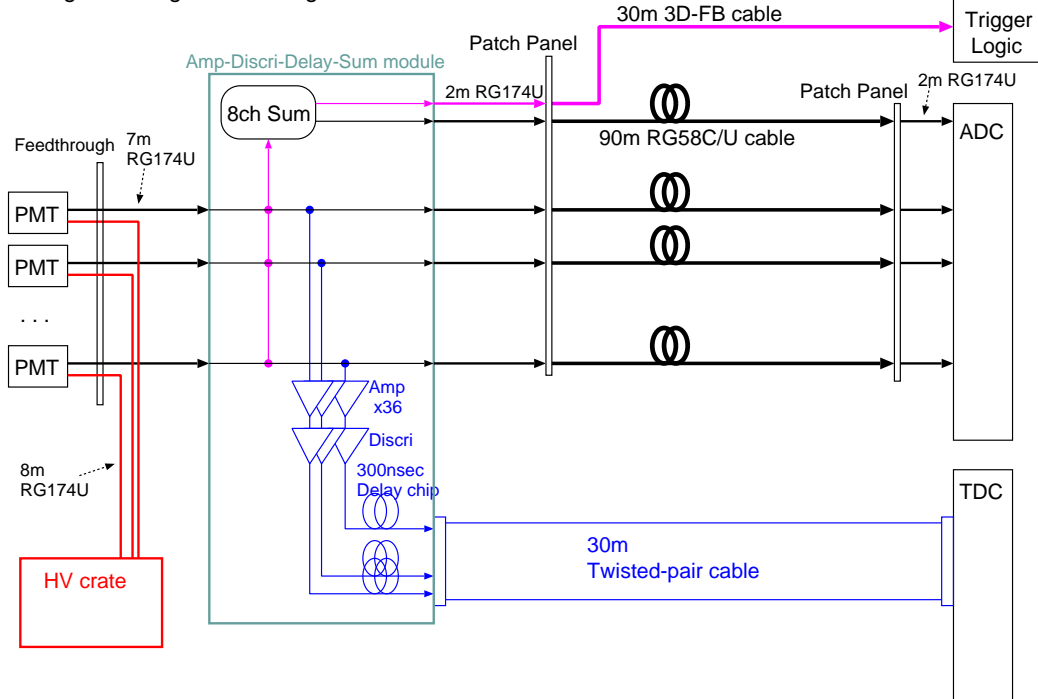


Figure 14: Cabling scheme for the charge and timing measurement.

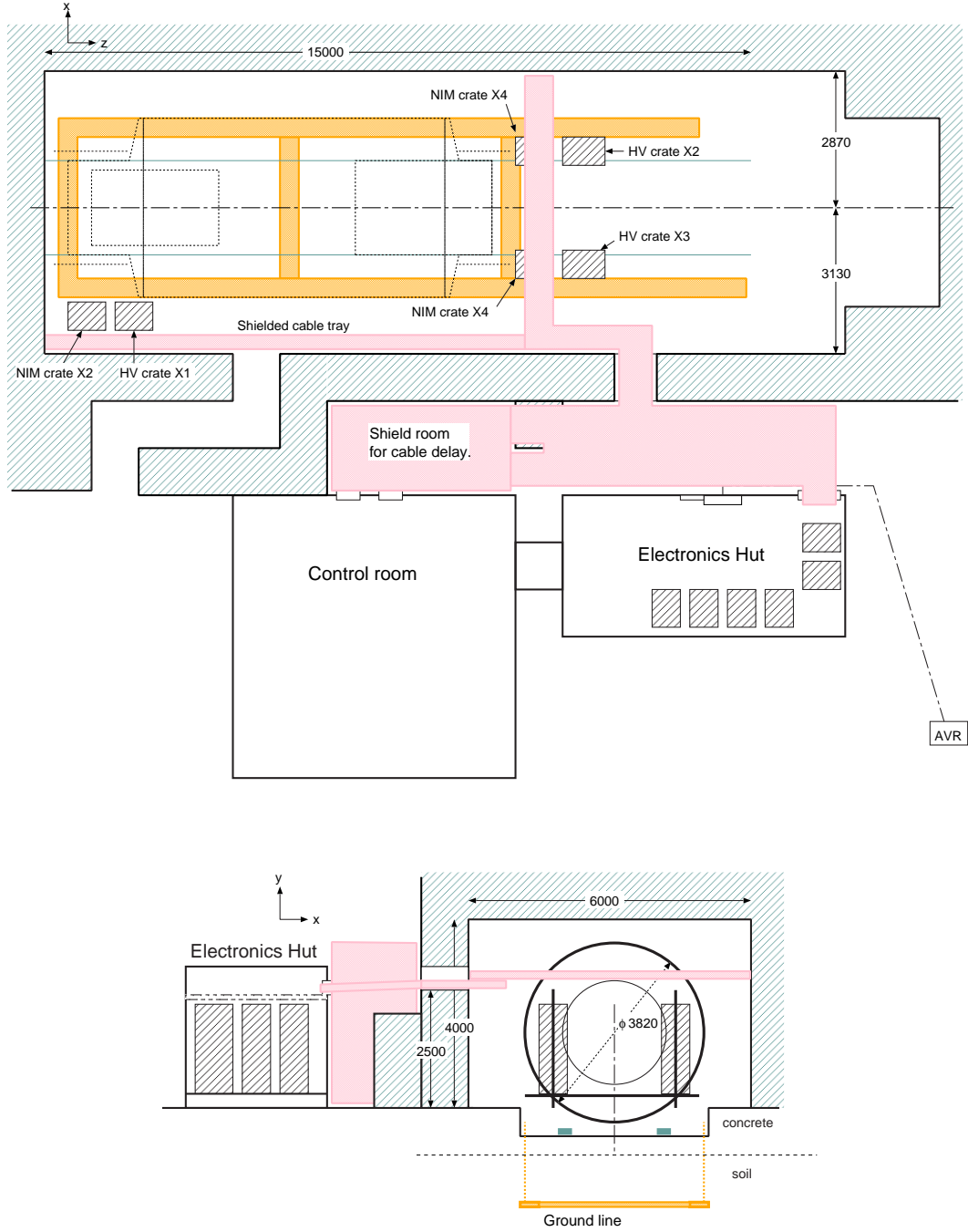


Figure 15: Signal cable tray and ground.

#### 4.11 Power-supply

For the input power-supply for the NIM, TKO, CAMAC and a part of the FAST-BUS, 100 V power-supply line is needed. For the rest part of the FASTBUS and CAEN HV system, 200 V  $1\phi$  line is needed. The air-cooling device, dehumidiater and the vacuum-pump requires the 200 V  $3\phi$  line. The AVR (Automatic Voltage Regulator) should be recommended for the power-supply in the viewpoint of the

stability. Due to some budgetary condition, we could only prepare the AVR for 100 V, and could not for the 200 V line. Two 100 V AVR's were used in the engineering run in 2002. Figure 16 shows the schematic view of the electric power-supply line configuration in the experimental area and the electronics hut.

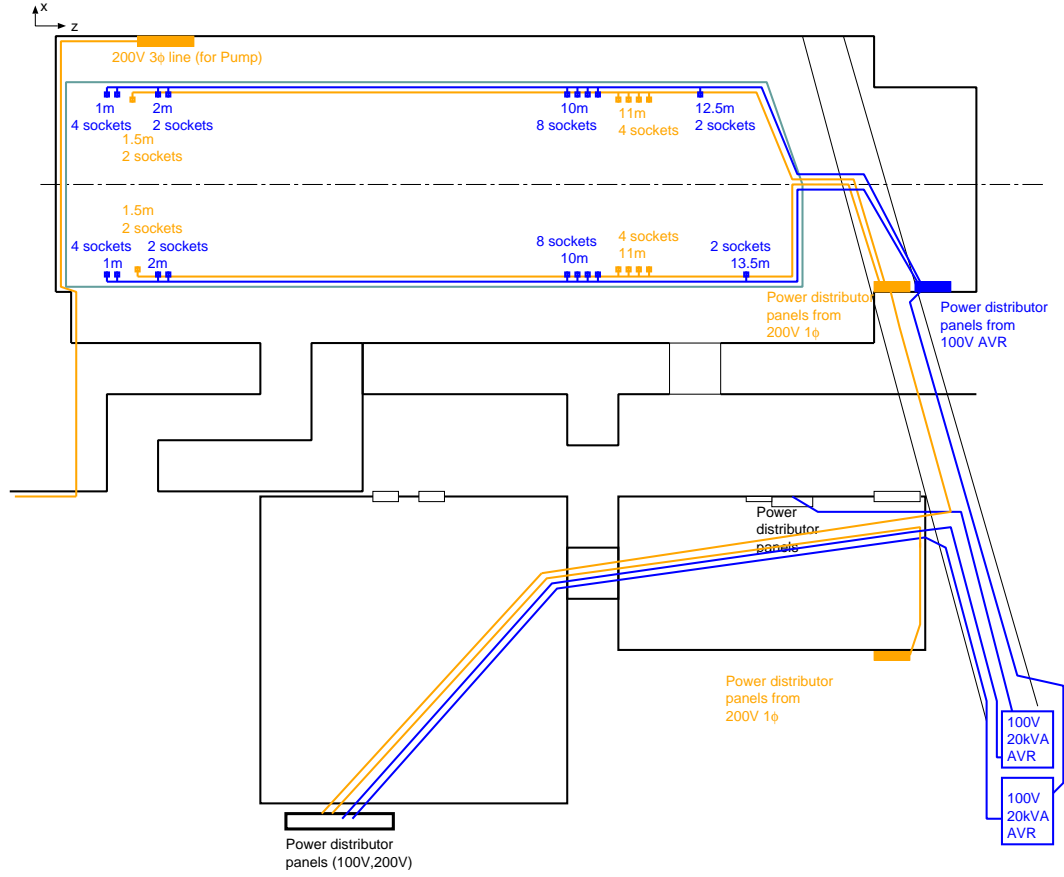


Figure 16: Schematic view of the electric power-supply line.

## 5 Computing environment

### 5.1 MIDAS as a base software

As is already mentioned in the Section 3.2, the network distributed system is used to construct the E391a DAQ system. The MIDAS software tool, which was originally developed at the PSI and TRIUMF experiment, was selected for the basic component of our DAQ system. It works on many platform including PC-linux, Sun Solaris8. Multiple frontend system with event-builder program is implemented in it.

### 5.2 Network

The private network was used for the DAQ computers so that they would not be disturbed by the transactions from other computers. This would lead the system to be safe and stable. The Giga-bit Ethernet was introduced in the private network so that even the 10 Mega-bytes of data per spill from three frontends would be transferred within less than a few hundred milliseconds during the beam off-spill time, which is short enough to accumulate the additional data like cosmic ray samples even during the two seconds of beam off-spill time. The gateway computer connects our private network to the KEK network in order to transfer the experimental data to the large storage system at the KEK central computing facility. This gateway plays a role of a firewall, and the computers on the KEK network cannot directly connect to our DAQ computers.

### 5.3 Frontend and backend computers

Four frontend CPUs, one for TKO-TDC system, two for FASTBUS-ADC, and one for High-Voltage system, are the diskless VME on-board CPUs. A Sun Solaris8 workstation works as a disk server for these CPUs as well as the network-boot server. This configuration gives us an easy maintenance of the large number of the CPUs.

One PC-Linux box is used as the backend server of the MIDAS system. The event-builder process which collects the data from three frontends together, the data-server process which distributes the collected data to the next stage of process, the data logger process which writes the data to the disk, and the run-control process to control the data acquisition, are running on this PC. A 180 GB of disk and a local DLT drive is attached to this PC as a local storage device.

One PC-Linux box is used as an on-line monitoring purpose. The event-display process which shows the real-time event sample time to time on-line, the event-checker process which checks the consistency of the data from three frontends, and a few event-monitors that shows the detector status or the triggering status or some important numbers related to the physics process by histograms, are running on this PC. The sampling data was distributed from the backend server via network.

Two Windows-PC are used for the environmental monitor. They keep working even when the DAQ was stopped, and keep logging the status of the environmental status.



## 5.4 HPSS as a mass storage system

The HPSS (High Performance Storage System) was employed as the large tape library system in the KEK central computing facility. This is a kind of a HSM (Hierarchical Storage Management). User can access the file on the tape just the same as the file on the disk seamlessly. The HPSS has several interfaces such as FTP, NFS, parallel FTP, Client-API or DFS. On the AIX system of our computing server, `ps.cc.kek.jp`, the most common and easy interface for us will be the DFS and FTP. The DFS system provide us the way to access the file on the HPSS as if it were on the normal file system. Since the maximum transfer speed with DFS is not so fast (about 5 Mbytes/sec at maximum), it is not suitable to read the large file sequentially. The FTP and PFTP to the HPSS data server provide us the good performance for the transfer of the large file at more than 20 Mbytes/sec of the transfer rate. The data file transfer from the DAQ data server PC to the HPSS data server was done by the FTP. All the network path between the DAQ data server to the HPSS data server has the Giga-bit speed, and we achieved about 15 ~ 20 Mbyte/sec of transfer speed during the engineering run in 2002.

## **6 Things to be updated**

### **6.1 ADC module**

As in mentioned in the Section 4.1.1, the LeCroy 1885N ADC has some deficit which restricts the data acquisition speed. Replacing the LeCroy 1885N with LeCroy 1885F, which has the same dynamic range but has shorter conversion time and block transfer capability, will increase the data acquisition rate drastically.

### **6.2 Trigger Veto timing**

In the engineering run in 2002, some of the timing from the veto-detectors are slightly delayed than expected, and that they could not completely kill the event to be vetoed at the trigger stage. One cause of this problem would be that the trigger-decision logic was not optimized well. It might be necessary to use the shorter cable for the veto detectors if they are used as the veto in the on-line trigger stage.

### **6.3 Fine adjustment of the timing**

The fine adjustment of the trigger-timing and the detector-hit timing between the detector channels was not well done in the engineering run in 2002.

### **6.4 Amp-Discriminator module**

The Amp-Discriminator module had some problem on its power consumption, stability and the noise on the linear-sum output at the engineering run in 2002. The detail is described in another note. These problem should completely be solved before the physics run.

### **6.5 200V AVR**

If the budgetary condition permits, it might be preferable to use AVR for 200 V power supply to the FASTBUS DC-power supply modules and CAEN HV crates.